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NONLINEAR METHODS FOR COMMUNICATIONS (U)

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Abstract Maximum 200 words

An innovative communication system has been developed. This system has the potential for improved secure communication for covert operations. By modulating data on the chaotic signal used to synchronize two nonlinear systems, they have created a Low Probability of Intercept (LPI) communications system. The researchers derived the equations which govern the system. Made models of the system and performed numerical simulations to test these models. The theoretical and numerical studies of this system have been validated by experiment (5,21-25). A recent design improvement has led to a system that synchronizes at 0 db Signal-to-Noise. This development holds the promise of a Low Probability of Detection (LPD) system.

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Nonlinear Methods for Communications - Final Report

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Chaotic Communications in the Presence of Noise

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Abstract

An innovative communication system has been developed. This system has the potential for improved secure communication for covert operations. By modulating data on the chaotic signal used to synchronize two nonlinear systems, we have created a Low Probability of Intercept (LPI) communications system. We derived the equations which govern the system. We made models of the system and performed numerical simulations to test these models. The theoretical and numerical studies of this system have been validated by experiment^{5,21-25}.

A recent design improvement has led to a system that synchronizes at 0 db Signal-to-Noise ratio. This development holds the promise of a Low Probability of Detection (LPD) system.

1.0 Introduction

This work has applied the fact that non-linear systems exhibiting chaotic behavior can be related to the investigation of a secure communications system. Chaos, with its noise-like properties, is useful as a mechanism for secure transmission of information. The dynamic behavior can be utilized to hide data and facilitate demodulation.

The general goal of this research is to apply results in nonlinear systems theory, particularly dynamical systems theory, to problems encountered in the design and analysis of communications systems. Specific paper objectives are to:

1. Demonstrate a practical Low Probability of Detection (LPD) communication system
2. Study the effects of noise, interference and distortion on chaotic communications systems
3. Obtain an understanding of the global parameter space of chaotic communication systems

A recent paper²² showed how two near-identical systems linked by a chaotic signal can synchronize with each other. Using two coupled loops, one stable and one unstable, as a transmitter of a chaotic signal, we showed that a third loop, nearly identical to the stable transmitter loop, can synchronize with that loop in the transmitter. The numerical study considered sinusoidal oscillators which are closely related to the well studied sine-circle

map. In an introductory experimental study of synchronized chaos we used a simple experimental DPLL to confirm our analysis.

In this paper we consider the transmission of data using the synchronous system. The problem is to design an Low Probability of Detection LPD^{18,20} chaotic communications system. The main reasons for using chaos in the communication circuit are the following:

- * the spectrum of the chaotic signals is noise-like,
- * the underlying structure of the chaos is useful in hiding data,
- * the parameters of the nonlinear system are useful as a "key"
- * Conventional spread spectrum has a basic "chip" rate that does not exist in the Chaotic Communications System

There are two general methods for using chaos in a communications system:

1. The chaotic generator is left unchanged by data during operation.
2. The chaotic generator is changed in some way by data during operation.

In method one, the information signal is added outside of the chaotic generator. An example of a system based on method one is signal masking. In signal masking a low power information signal is added into the spectral envelope of a chaotic signal. The higher power chaotic signal then literally masks the information signal.

In method two, the information signal is added *inside the chaotic generator*. The data is intrinsically contained within the chaos. We have selected method two because it yields the best LPD communications system utilizing nonlinear dynamical systems theory.

Example data modulation techniques for method two are as follows:

1. The chaotic system parameters can be changed between two discrete states.
2. The chaotic signal can be multiplied by a binary signal.
3. The chaotic signal can be converted to two discrete states which is then multiplied by the binary signal. The mixed signal is then converted back to an analog signal.

Not all of these methods hide the data. The last alternative offers the best protection from interception. This is because the binary data is mixed in an intricate way into the chaos itself.

1.1 Comparison to Other Research

In this section we will discuss related research and how our work differs. For the sake of brevity we review only a small sampling of the references in the applicable fields.

Pecora and Carroll's work^{16,17} is based on the idea that a chaotic system may be decomposed into two subsystems; namely a stable subsystem and an unstable subsystem. The stable subsystem can then be replicated and driven by the unstable subsystem. The two stable subsystems then have identical outputs after transients have died away. M. de

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Sousa Viera has shown that the Lyapunov exponent for the subsystem is the same as the Lyapunov exponent of the entire system. This means that the entire system can be studied, without breaking it up into subsystems.

Pecora and Carroll^{16,17} also suggested a data communications system which is inherently noise sensitive. The information signal is outside of the chaotic generator. The information signal is at one-fifth the power of the chaos when sent over the channel, and the frequency spectrum of the chaos envelopes the frequency spectrum of the signal. Although their schemes work with little or no noise it would be extremely difficult to make them work with even 20 dB SNR.

A. Oppenheim¹⁵ is pursuing the use of chaotic signals for masking information-bearing signals and as modulating waveforms in spread spectrum systems. The synchronized chaos uses the same structure as Pecora and Carroll. The transmitter is a Lorenz system and the receiver is a subset of this system.

Both of these approaches differ from our approach of selecting the stable and unstable parts of the chaotic circuit. We simply take two circuits and connect them together. One of the circuits operates unstably and the other is stable. We then just replicate the stable circuit to act as a receiver. Our method allows one to add more unstable components to increase the dimensionality of the chaos whereas the other research approaches do not. Filters, limiters and data modulation circuits can be added to the basic chaotic circuit to provide robust performance in low SNR environments. Our modulation technique is totally different. We make slight changes to the chaotic circuit itself in such a way as to not give away the fact that we are modulating data. We then only have to compare for degrees of synchronization between two signals. In this way we can tolerate much more noise.

2.0 Communications System Design

Our focus is on the areas of LPD communications systems, the communications applications of chaotic phenomena and synchronization. In the rest of this section we describe problems that arise in these applications.

2.1 Problems in designing Communication systems using Chaotic phenomena

Several problems have been found in designing chaotic communication systems. Some of these problems are as follows:

1. Adding noise to a synchronized chaotic system can cause loss of synchronization.
2. Global system behavior is impacted by the addition of filters, VCOs with sin wave outputs, VCOs with triangular wave outputs and other components changes^{5,21-25}. This implies that communications engineering must consider the implications of nonlinear dynamics on each system change.

3. How should the communications system transmit two parts of the chaotic signal without distortion?
4. How does the system design compensate for amplitude variations caused by the channel? Adding a limiter can change a chaotic system into a system that doesn't exhibit any chaotic behavior, i.e., multiply periodic. This implies that the system can lose its "noise-like" behavior desired for LPD.
5. How does the system design modulate data in a way that is hard for the interceptor to detect.

The first two problems are the general LPD problems. Problems 3-5 are specific problems which we solve in the next sections.

2.2 Distortion free multiplexing

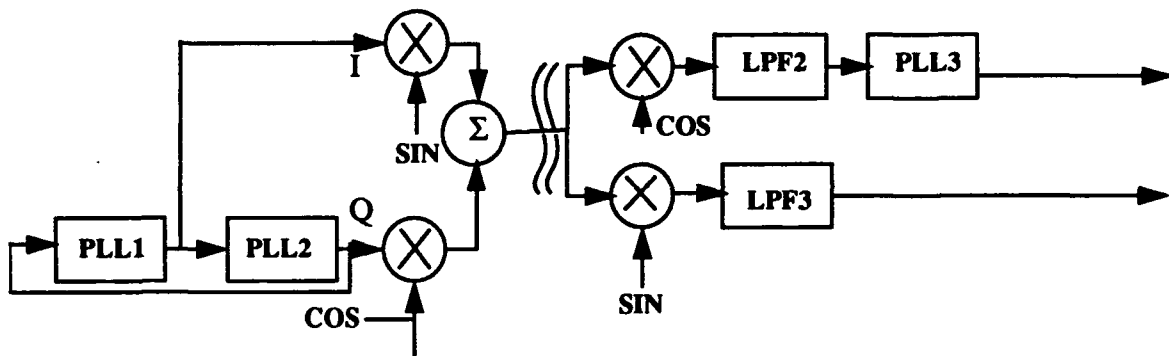


FIGURE 1. The original secure communications system

The first problem solved is how to transmit both the I and Q chaotic signals. The two signals, illustrated in Figure 1, were needed by the receiver to tell when the system is synchronized. Quadrature multiplexers and demultiplexers were used to transmit the two signals. This multiplexing and the channel required the use of low pass filters. The low pass filters, LPF2 and LPF3 caused both amplitude and phase distortions.

Originally, high-order Finite Impulse Response (FIR) filters and an Automatic Gain Control (AGC) mechanism were added in an attempt to provide multiplexing free of distortion. The FIR filter minimized phase distortion. The AGC compensated for amplitude variation. The result was that even small distortions in the filter degraded system performance.

Filters were then added in the appropriate locations and the feedback loop altered in the design such that equal distortion effects occur in the transmitter and in the receiver. This system is illustrated in Figure 2. The two low pass filters LPF2 and LPF3 were necessary to eliminate the double frequency component of the demultiplexed signal. The filter LPF1 was added to precompensate for the distortion caused by LPF2. LPF4 was added to compensate for the distortion caused by LPF3. Now the use of IIR filters was possible because the distortion effects were compensated. The system was synchronized because the input to PLL3 was the same as the input to PLL1.

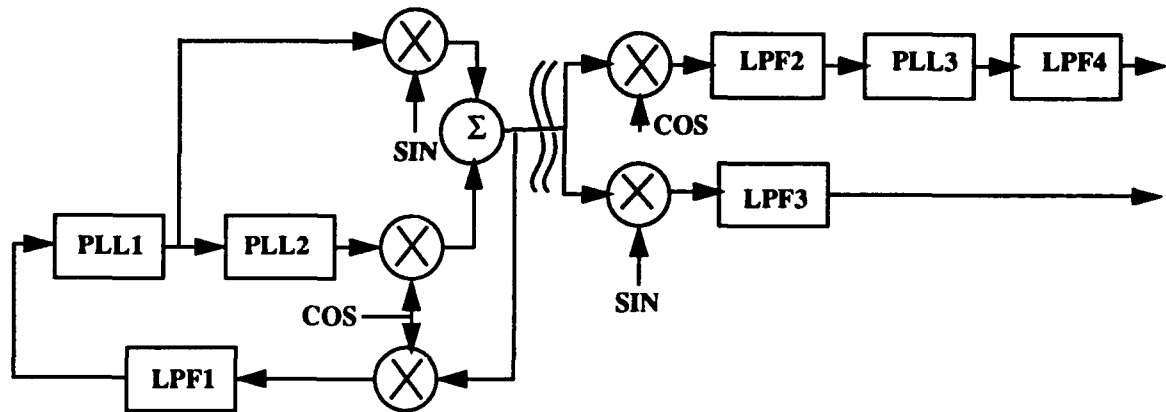


FIGURE 2. The secure communications system with filter in the signal generator feedback path.

2.2.1 Removing amplitude variation without eliminating chaos

The second problem was amplitude variations caused by the channel. The system of Figure 2 was still sensitive to amplitude variation of the received signal. A static amplitude error between the input to PLL3 and the input to PLL1 caused the output signals of these two phase-locked loops to be out of synchronization.

The problem of amplitude variation was solved by inserting a hard limiter and VCO in front of PLL3 in the receiver. The hard limiter eliminated the dependence on amplitude at the input of the receiver completely. The square wave output of the limiter was converted into a sine wave by use of a VCO. These components allowed the transmitter to still produce chaos.

The limiter outputs two voltages: V_1 when the input was less than zero, and V_2 when the input was greater than zero. We now have an eight dimensional parameter space. The parameters are the center frequencies, loop gain, and offset voltages of PLL 1 and 2, and the limiter output voltages V_1 and V_2 . Each one of these parameters can be used as part of a "key".

The improved system is shown in Figure 3 and 4. The receiver has matching elements to the transmitter. The PLLs 1 and 2 are identical, and the LPFs 1 and 2, 3 and 4 are identical. The hard limiters and VCO's are identical in the transmitter and the receiver. Also the transmitted reference and information signal go through the same elements in the same order.

FIGURE 3 The improved Transmitter with limiters to remove amplitude sensitivity.

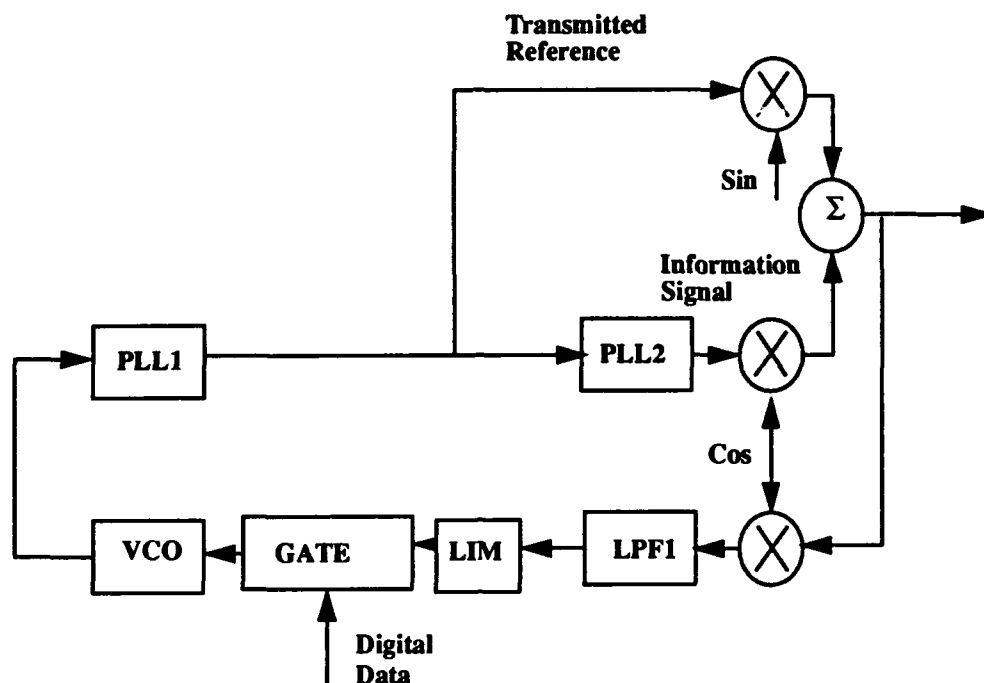
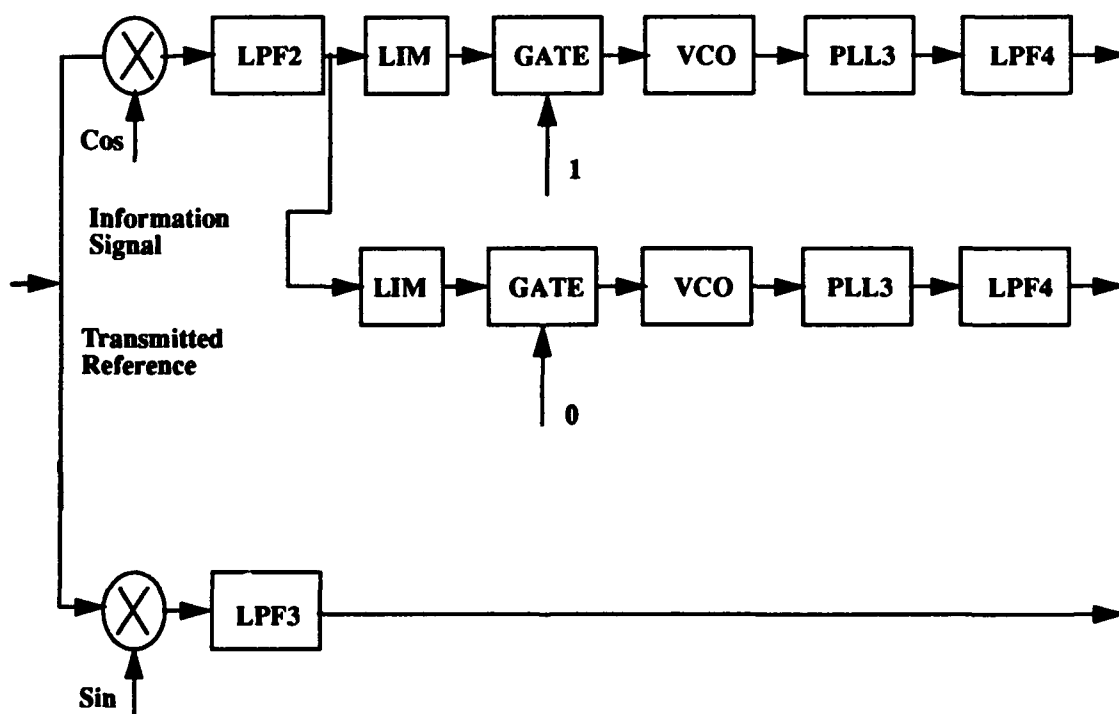


FIGURE 4. The improved Receiver Synchronization Circuit



The nonlinear dynamics of this new system was examined next. There was no guarantee that the new system would operate chaotically and synchronize. In fact it was found in our previous studies of analog PLL's¹⁹, that inserting hard limiters into a chaotic system had a tendency to eliminate the chaos. Analyzing the system with nonlinear dynamics tools showed that the system was still chaotic. The results are illustrated as follows: signal spectrum, Figure 5, the bifurcation diagram, Figure 6, the global synchronization, Figure 7, and the synchronization between transmitted and recovered signals, Figures 8 and 9.

The signal spectrum at the output of PLL2 is illustrated in Figure 5. The power was broadband and noise-like. This was an indication that the signal was chaotic.

FIGURE 5 Spectrum of PLL2 output.

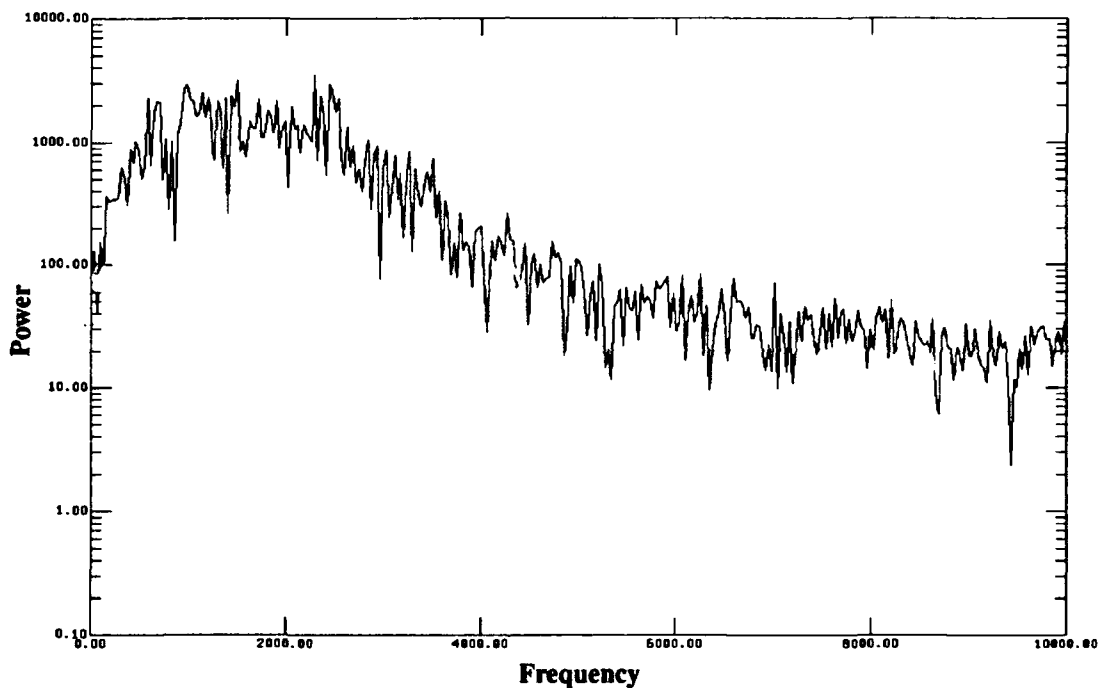
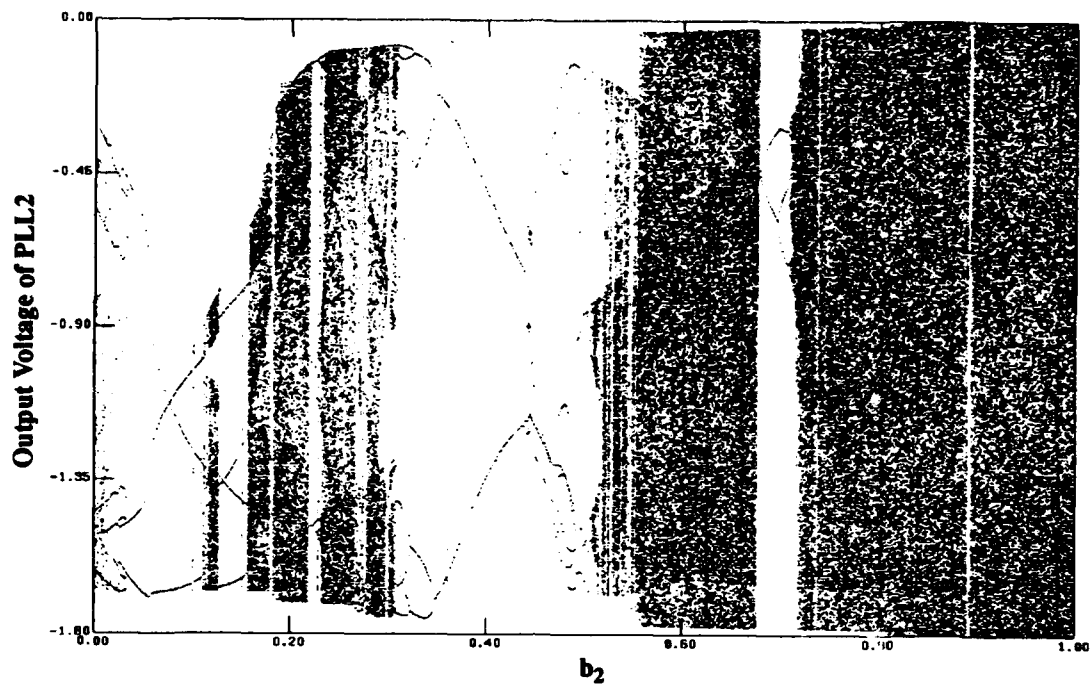


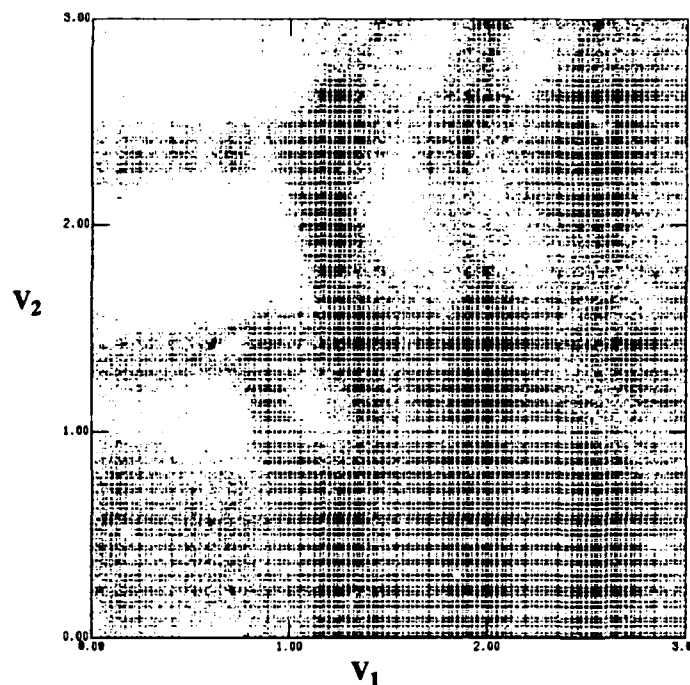
Figure 6 is a bifurcation diagram with the parameter b_2 (offset voltage of PLL2) plotted against the output voltage of PLL2 at the sampling time of PLL1. The other parameters are constant at $b_1 = 0.4$, $V_1 = 2.2$, and $V_2 = 2.3$. For each b_2 value, 400 voltages are plotted. The bifurcation diagram indicated that the system could operate in a chaotic mode.

FIGURE 6 Bifurcation Diagram for improved secure communications system.



A global synchronization plot, illustrated in Figure 7, is for parameter values of $b_1 = 0.4$, $b_2 = 0.95$, and for various values of the limiter voltages V_1 and V_2 . It is seen from Figures 5 that the system was operating in a chaotic mode and yet the outputs of the LPF3 and LPF4 were in synchronization when $V_1 = 2.2$ and $V_3 = 2.3$.

FIGURE 7 Global Synchronization Plot



The effects of noise was examined next. A simulation was run at 20 db SNR. Figure 8 was the result, it showed that near perfect synchronization was obtained. Figure 9 showed how well synchronization occurred with SNR = 0. This obvious synchronization behavior for a chaotic signal with equal amounts of white Gaussian noise is what leads us to believe that an LPD system is feasible.

2.3 Data Modulation

The third problem solved was how to modulate data in a way that is hard for the interceptor to detect. This system provided a very convenient way to modulate data onto the chaotic signal. The digital data was modulated onto the chaotic signal by treating the output of the hard limiter as digital ones and zeros. A gate mixes the signals by using an exclusive-nor circuit. The mixed signal is then converted to an analog voltage before being fed to the VCO. The data was placed in a hold circuit so that data transitions occurred only when the hard limiter output changed state. It is this use of the dynamic structure which makes the data rate difficult for an interceptor to detect. Many more limiter transitions should occur than data transitions in order to eliminate the effects of transients. Many more limiter transitions than data transitions helps stabilize the bit rate. In this way the data transitions are lost in all of limiter transitions.

FIGURE 8 Synchronization with 20dB SNR.

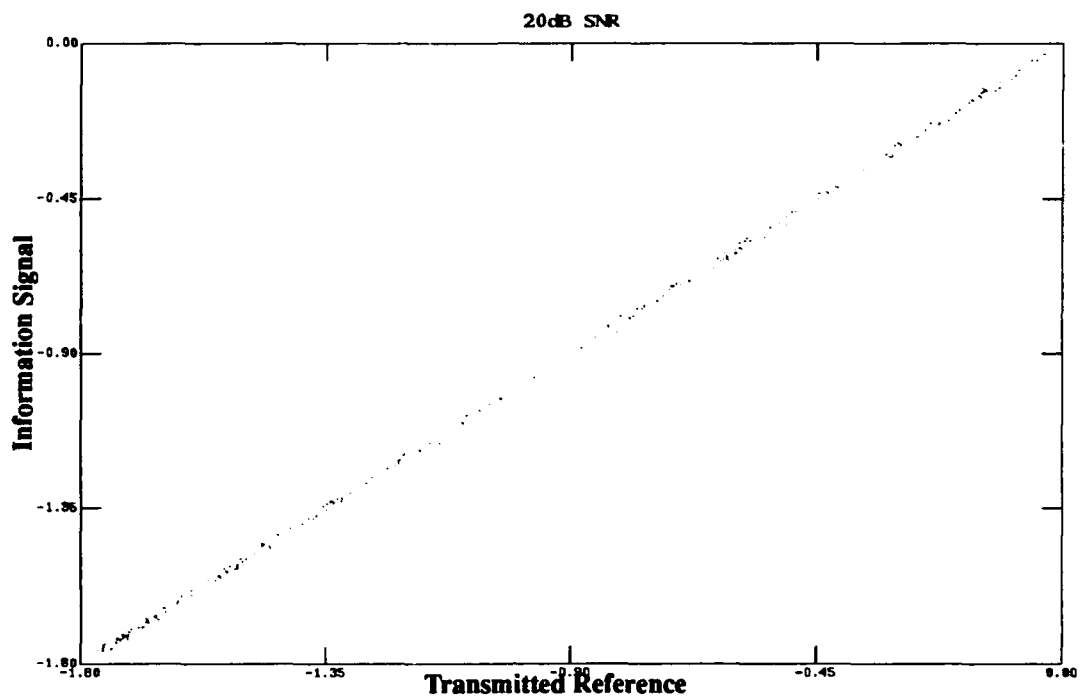
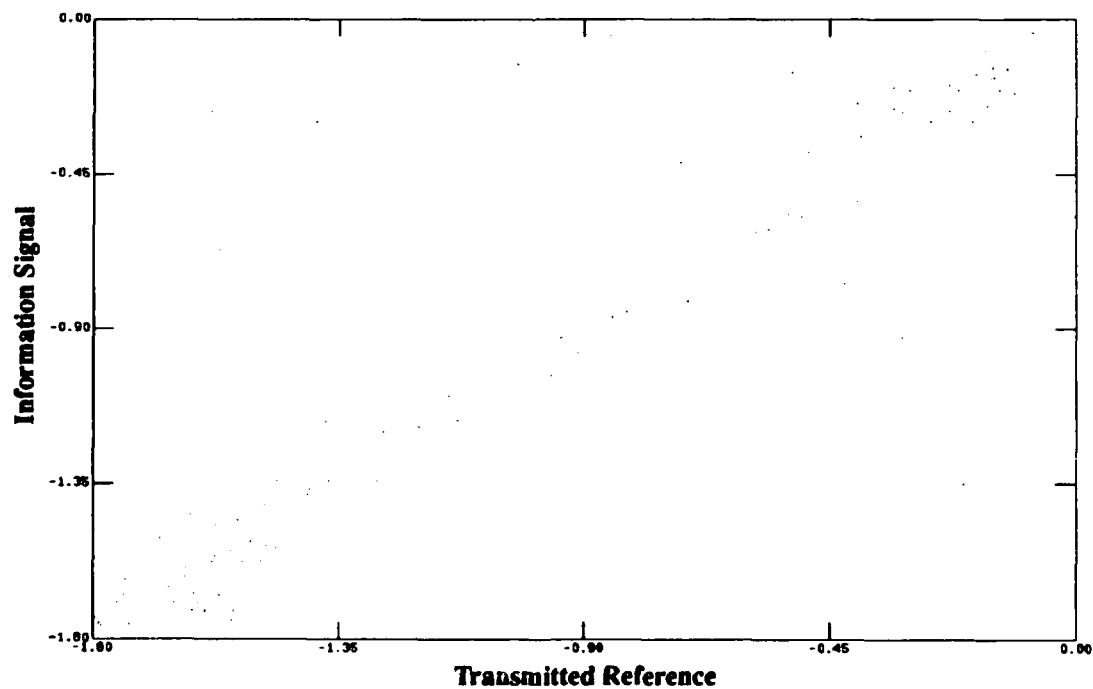


FIGURE 9 Synchronization with 0dB SNR indicates an LPD secure communications system



3.0 Conclusions

We have solved three major problems dealing with making a realistic communications system using chaos. There are several more that we know about.

Our single largest problem is how to reduce the Signal-to-Noise ratio. A related problem is determining whether the transmitted signal can be detected by non-standard means. These problems are related because their solution resides in the ability to get a clear look at the transmitted signal. The solutions here might come from Empirical Chaos⁸⁻¹¹, Higher Order Spectra¹⁴ and Wavelets⁴.

Another problem is that a bit synchronizer and bit detector need to be designed. This is challenging because the modulation techniques used make the data rate chaotic. Standard communication engineering techniques, however, should solve this problem.

The problems of multipath and cochannel interference must be addressed. These problems motivated are solution to the amplitude variation issue. Additional sensitivity studies are needed.

4.0 Acknowledgments

We thank M. Steinberg, J. Huang of Loral and M. A. Lieberman, A.J. Lichtenberg, and M. de Sousa Vieira for many helpful discussions. This research was supported by ARPA Grant W-SO-242614-T-12/91.

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Non-linear Methods For Communication

1.0 Executive Summary

This is the first annual report on Non-linear Methods For Communication. During the past year we have performed experiments, run simulations, and done analysis on several different aspects of secure and high speed communications systems using the methods of non-linear dynamics.

In the area of secure communications we have investigated system using chaotic circuits for the creation of low probability of intercept (LPI) communications. The system we considered is the synchronization of a receiver, composed of one or more digital phase lock loops (DPLLs), to a transmitter, also composed of DPLLs, which is transmitting a chaotic signal. We have explored the possibility of digital data transmission with such a system. The results hold great promise for the creation of a tactical LPI communications system. We have also explored an alternative method of generating pseudo random noise (PRN), using the chaotic behavior of a system of DPLLs, for use in existing spread spectrum systems. The work to date has shown the properties of a circuit operating in the chaotic mode is suitable for the creation of PRN.

In the area of high speed communications we have simulated the behavior of a second order analogue phase lock loop containing a hard limiter. The results of the simulation have validated the linear analysis usually done for such systems and has explored parameter regions where the system behaves chaotically.

In the area of synchronization of networks we have begun the study the synchronization of many coupled DPLL's to a common frequency. Such devices may be used as synchronization elements in networks of clocks, power generators, microwave systems, satellite systems, and computer networks.

1.1 Purpose of the effort

The general goal of the research is to develop more effective methods for predicting communication systems performance through the application of methods of non-linear dynamics. The motivation for this work may be considered to lie in the following areas: Secure Communications which includes LPI communications for covert applications and new Milstar waveforms for tactical communications, high speed communications which includes DARPA High Performance Computing Program, DARPA Strategic Computing Program, and the Federal High Performance Computing and Communications Program, and finally network synchronization which involves Code Division Multiple Access (CDMA) requirements for system synchronization and timing and LightSat Systems which require self-synchronization in tactical applications.

This goal is embodied in a two pronged effort:

1. The study of synchronization in systems useful for communications purposes using the methods of non-linear dynamics
2. Transfer of the knowledge of the techniques of non-linear dynamics to engineering community studying communications systems.

1.2 Organization of the report

This report is organized as follows: Section two describes the organization of the research, including the names of the people involved in performing it, and supplies a summary of the work performed to date including technical results, conclusions, and the implications for further research during the coming year. Section three contains reports of the research written by the individual researchers. These reports are detailed and technical in nature.

2.0 Organization of the research

The research group on non-linear methods for communication is divided into two sub-groups. One sub group is at the University of California at Berkeley (UCB) and the other is at LORAL- WDL. Each sub group brings its own special virtues to the project.

Loral understands practical communication systems but is new to non-linear dynamics. Thus it provides guidance on communications issues and concerns itself with problems directly related to realistic communication engineering questions. The sub group at U.C. provides the expertise on non linear dynamics and develops the more theoretical aspects of the study. The two sub groups also have different experimental capabilities. The resources of both groups are complementary.

The members of each subgroup pursue different aspects of the research. In order to insure that there is sufficient technical guidance and to decide on new directions in the research the two sub groups have formal meetings every four weeks. In addition the E mail facilities available to the group members are exploited to exchange technical information. Table 1 contains the names of the members of the research group, which subgroup they are a member of the role they played in the performance of the research, and the section which contains a report of their work.

2.1 Summary of the research projects

Figure 1 is a graphical representation of the tasks performed during the contract year. The efforts may be divided up into four areas. Secure communications, in turn subdivided into standard and non standard methods, high speed communications, and network synchronization.

2.1.1 Secure Communications

Under the heading of secure communications work was performed in two areas; what may be termed non standard methods and Spread Spectrum.

TABLE 1. Personnel Of Research Group And Their Responsibilities

Name	Group	Responsibility	Section
R. Sherman,	LORAL	guidance on communication issues	
Prof. A. J. Lichtenberg	UCB	guidance on non linear dynamics	
Prof. M. A. Lieberman	UCB	guidance on non linear dynamics	
M. de Sousa Vieira	UCB	analysis and numerical simulation of synchronizing systems	3.1,3.2 & 3.9
W. Wonchoba	UCB	derivation of mapping eqns	3.3
J. Gullicksen	LORAL	experimental work confirming synchronization and simulation of realistic communication system	3.5
P. Khoury	UCB	experimental work confirming bifurcation diagram	3.6
Prof. J.Y. Huang	LORAL	simulation of data transfer	3.4
		simulation of PN generation	3.7
M. Steinberg	LORAL	simulation of analogue PLL	2.0,3.8

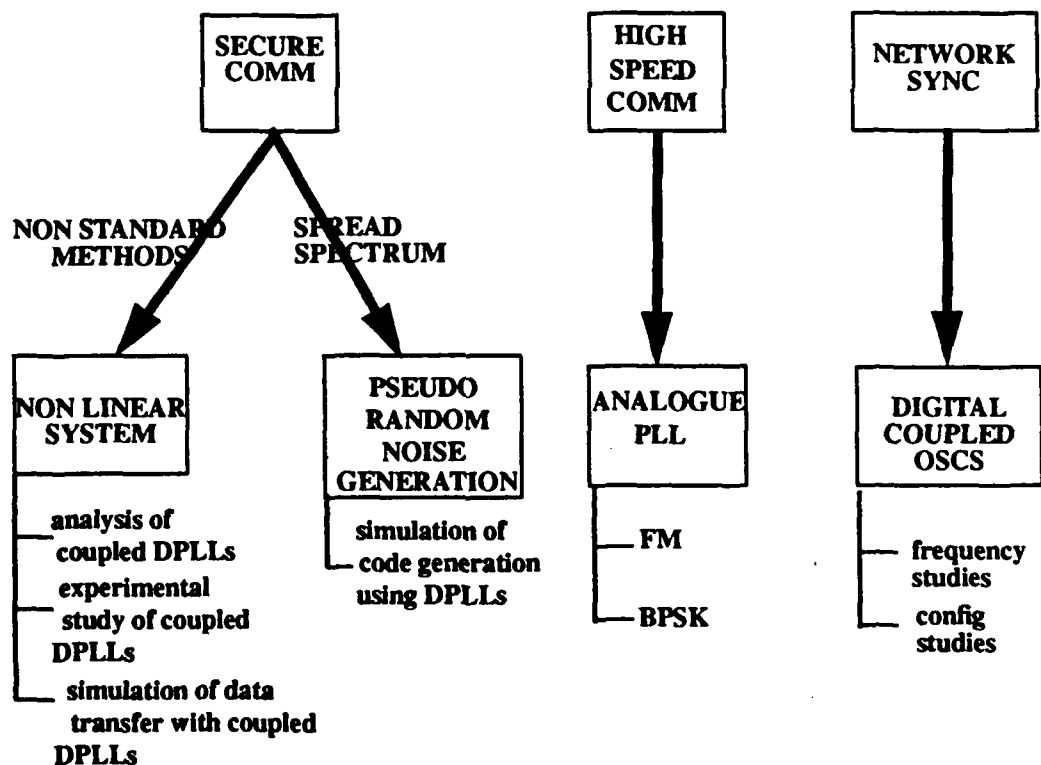


FIGURE 1. Results of First Years Tasks

A. Non Standard Methods

The work on non standard methods for secure communications involved the investigation of non-linear systems which used DPLLs (see figure 2 for a block diagram of a DPLL). The efforts involved analysis, experiment and numerical simulations. We showed that the concept of synchronized chaos, introduced by Pecora and Carroll, can be applied to coupled DPLLs.

In particular we applied the idea of chaotic synchronization to a system which consisted of three or more coupled digital phase locked loops. We were able to show that the dynamics of such a system is far more complicated than that of a single loop, which is governed by a one-dimensional circle map. In the case of two coupled loops, we observed that the dynamics is governed by explicit mapping equations only for certain regions of the parameter space. In the regions for which mapping equations can be derived, we found the universality class of the coupled loops.

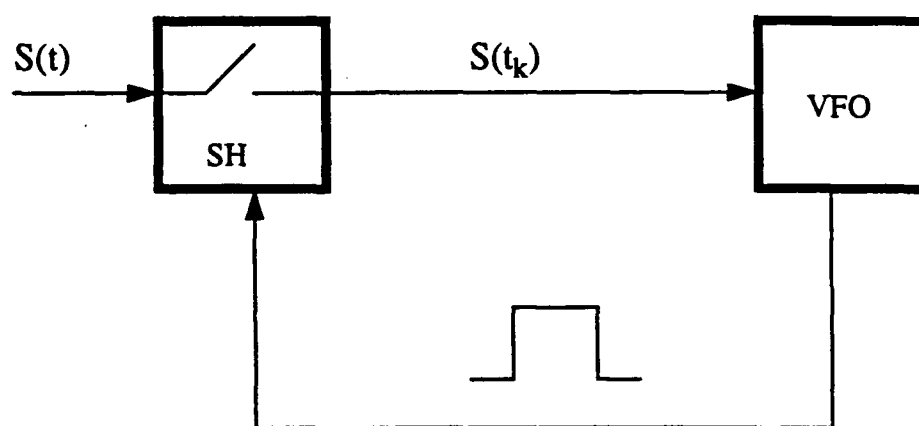


FIGURE 2. Schematic diagram of a DPLL

Using non linear analysis techniques such as the generation of surfaces of section (i.e., Poincare Maps) as a functions of system parameters, bifurcation diagrams, and calculation of Liapunov exponentials we analyzed a model communications system which was made up of DPLLs. The chaotic carrier was generated in a subsystem of two or more digital phase locked loops, where one subset of loops is stable and the other is unstable, i.e., their Liapunov exponents are negative and positive, respectively. The receiver consisted of subsets of stable loops only. Both a modulated chaotic carrier and a chaotic synchronization signal can be transmitted. We verified numerically that the receiver does synchronize with the transmitter if the stable subsets of loops in the transmitter and receiver are identical. We studied the phase space where synchronization occurs, and quantified the degree of synchronization using the concept of mutual information (This work is described in detail in sections 3.1 and 3.2).

Further analysis of the problem led to a derivation of mapping equations for the coupled DPLL system. We showed that these equations, and hence the dynamics of the coupled DPLLs, are generalizations of the dynamics of a bouncing ball on a large periodically-vary-

ing table, a system which has been studied by several authors. We showed that no fixed points exist in this map, but that period-two points do exist. (See section 3.3 for details)

The results of the numerical analysis were verified by experiments. One experiment demonstrated the synchronization of the "receiver" and "transmitter" in the model communication system. Even though no particular care was taken to assure that all parts in the receiver and transmitter were matched the experiment confirmed the values of the parameters for which the synchronization occurred. (see section 3.5) The other experiment traced the bifurcation behavior of the system and provided an experimental verification of the numerically produced bifurcation diagram (see section 3.6).

In order to further explore the possibilities of using the synchronization to a chaotic signal for communications purposes two more numerical simulations were performed. The first simulation examined a transmitter made up of two coupled DPLLs and a receiver made up of two coupled DPLLs (see figure 3 "Parameter Matching Circuit"). The second DPLL in the transmitter has its coupling coefficient set very high so that the loop has a positive Lyapunov exponent; the coupling coefficient for the first loop in the transmitter is made to take on two different values, one value for the binary digit of 1-bit and another value for 0-bit (both values of the coupling coefficient are chosen so that the loop has a negative Lyapunov exponent). The output of the voltage controlled oscillator of the second DPLL is transmitted to the receiver where it acts as the inputs to both DPLLs. The difference between the two DPLLs making up the receiver is in their coupling coefficients. The coupling coefficient for one of the DPLLs matches that for 1-bit used for the first DPLL in the transmitter and that for the other DPLL matches that for 0-bit. Hence, when a 1-bit is transmitted, the output of the first DPLL in the transmitter will be in phase synchronization with one of the DPLLs in the receiver and when a 0-bit is transmitted, it will be in synchronization with the other. The result of the simulation suggest that in order to have a bit error probability on the order of 10^{-6} or lower, the input SNR must be much higher than twenty (20) dB, which is almost one order of magnitude higher than the case of BPSK or QPSK signalling system. Hence, this digital data transmission system may be considered a LPI (low-probability of intercept) communication system, but its power efficiency is very poor. (For details see section 3.4)

The second simulation, which is still underway, involved the creation of the model of a realistic and realizable communications system using the coupled DPLLs. In the system described in the previous paragraph the output of first DPLL in the transmitter is not available at the receiver. Thus the decision variable used at the receiver for the detection of the binary data, must be based on the received signal (which is the output of the second DPLL in the transmitter) or certain variables related to the two DPLLs in the receiver. This decision variable must be such that the 1-bit or 0-bit embedded in the received signal can be extracted without any ambiguity in the absence of input thermal noise. An alternate procedure is to have a communication system using chaotic signals as the transmitted symbols. The system consists of two coupled digital phase lock loops (DPLL's) acting as a transmitter, a modulator, a channel, an additive noise source, a demodulator, and a DPLL acting as a receiver. (see figure 4 "Transmitted Reference Circuit")

The coupled transmitter operates in a region such that its output is chaotic. The receiver then takes in this chaotic signal and synchronizes to it. The results to date indicate that when the modulator/demodulator were added without doing carrier recovery that synchronization was lost. (The details are to be found in section 3.5).

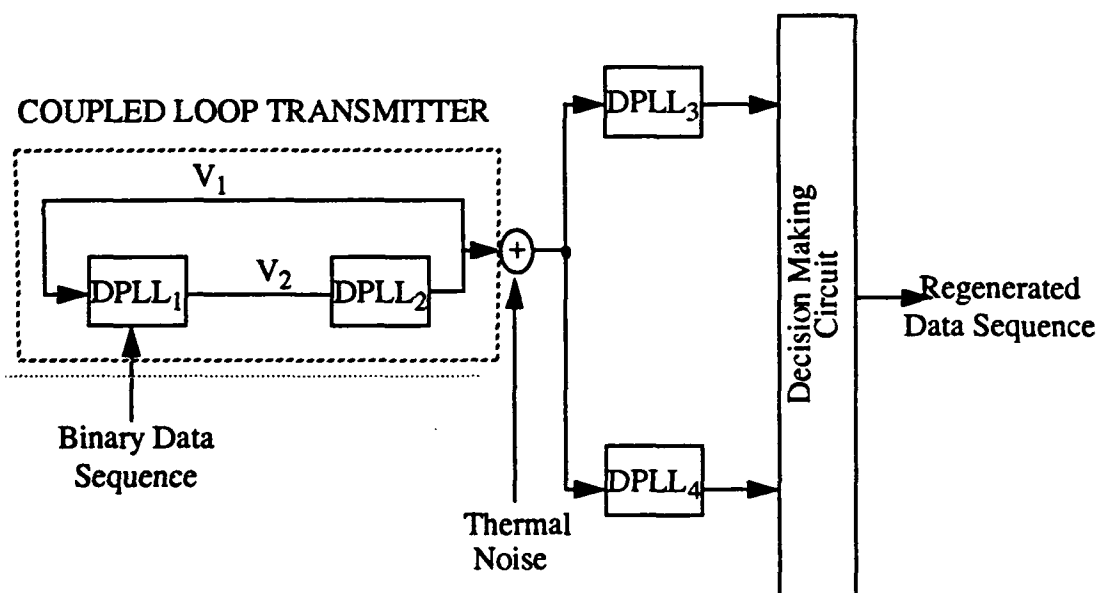


FIGURE 3. Parameter Matching Circuit. A Digital Communication System Employing Coupled Digital Phase Lock Loop With The Second Loop Having Positive Lyapunov Exponent

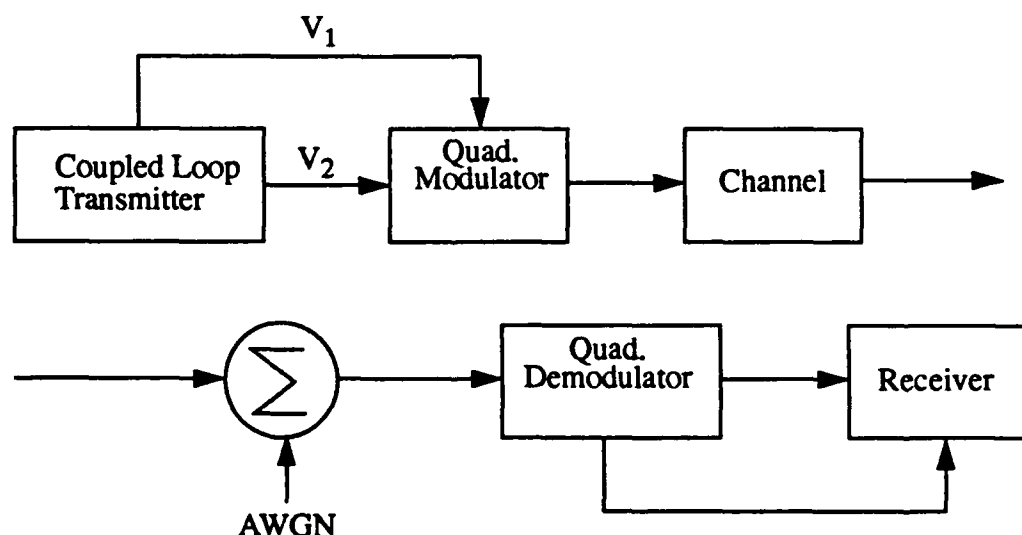


FIGURE 4. Transmitted Reference Circuit. Block Diagram of General Communication System Using Coupled Loop Transmitter

The results of the analysis, experiments and simulations related above, and described in detail in section 3, suggest that synchronization to chaotic signals may provide one possible solution to the problem of LPI communications. In order to further explore this idea the group intends to pursue the following courses of action during the coming contract year.

We will continue the exploration, through simulation, analysis and experimentation, of the periodic, quasiperiodic and chaotic regimes of DPLLs as well as their transient behavior. The concept of mutual information to quantify the degree of synchronization between loops when they are not identical will continue to be used. The studies already underway will be augmented by the use of symbolic dynamics, fractal dimensions, etc. We also plan to study chaotic synchronization in more complex systems, since these may be necessary for practical implementation. One of our priorities will be to work on modulation techniques for the transmission of information. Further work will be undertaken to find the optimal decision variable for parameter matching system. Finally to effect the appropriate design of filters for use in circuits involving chaotic signals we will explore the higher order statistical characteristics of chaotic signals.

B. Spread Spectrum

In spread spectrum systems, the pseudo-noise (PN) codes needed for signal spectrum spreading are, in general, generated from n-stage shift registers with either linear or non-linear feedback. It is obvious that the sequence generated by the n-stage shift register with feedback is periodic whose period can not be longer than $2^n - 1$. The number of linear logic functions yielding the maximum period is $2^{2^n - 1} / 2$ when non linear feedback logics are used. We simulated a circuit consisting of N first order DPLLs connected in a ring configuration with one of the DPLLs having a positive Lyapunov exponent. (see figure 5 -in our case N took on the value of either 2 or 4.) The output of any one of the DPLLs in the circuit can then be sampled at a rate equal to a small fraction, say 0.1, of the nominal frequency of the DPLL's, and each of the samples are quantized into a binary digit of 1 or 0, depending on the sample being positive or negative, respectively. The binary sequence so generated has the potential of being truly random with a period which is very long. We constructed an algorithm by which two identical circuits can be brought into synchronization, both for the clock signals and code phases.

The results of the simulation are that properties of these sequences, including statistics on 0/1 balance, auto-correlation and cross-correlation between sequences meet the requirements of pseudo noise generators. (The details of this work are reported in section 3.7)

A larger collection of sequences generated using the system with different number of DPLL's in the systems and with different coupling coefficients needs to be studied, so as to be certain that the codes sequences generated by the systems have all the desired properties. The periods of the generated sequences must be determined either through theoretical investigation or by simulations, possibly using the techniques of cell to cell mapping. The effects of using a shorter word length in the arithmetic operations, on the properties of sequences being studied, also require further investigation.

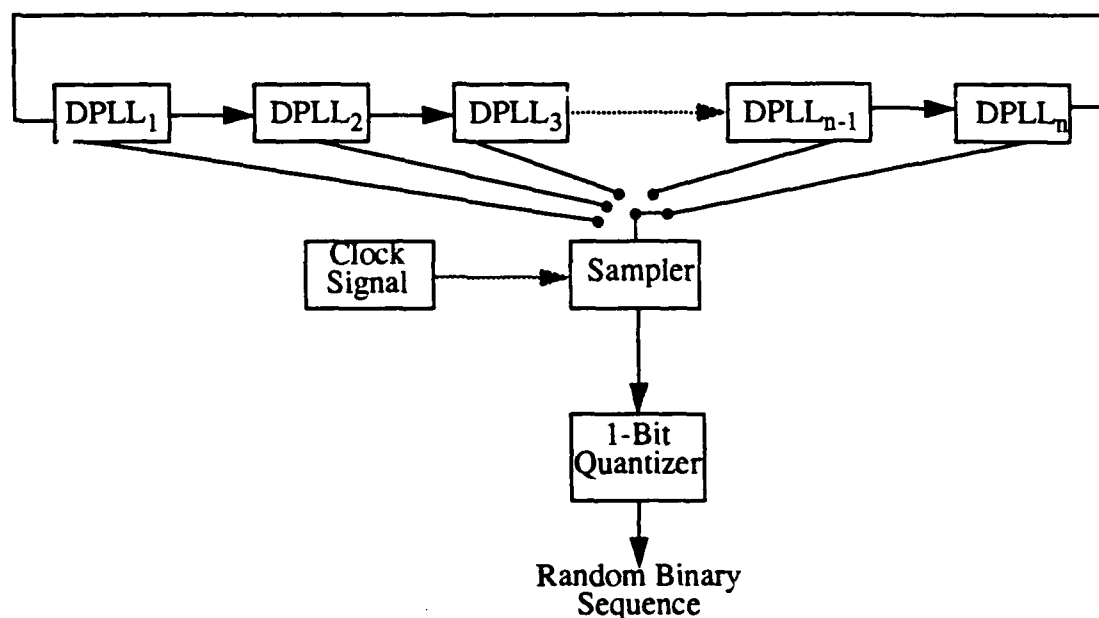


FIGURE 5. Pseudo-Noise Sequence Generator Employing N Digital Phase Locked Loops (DPLLs) Connected in Ring Configuration With the n-th DPLL Having Positive Lyapunov Exponent

2.1.2 High Speed Communications

Phase locked loops (PLLs) are useful for phase and frequency, synchronization. An independent study at LORAL WDL explored possibilities for high speed data recovery using an analogue phase lock loop which contained a hard limiter. A linear analysis indicated that the such a loop showed great promise. However, since the behavior of a phase lock loop with a hard limiter in it was not well understood it was decided that an analysis of a system containing a hard limiter should be performed using the methods of non linear dynamics. The non linear analysis confirmed the results of the linear analysis for FM in the region where the loop is normally operated. In addition it showed that the hard limiter introduced chaos in regions of operation of the PLL where there is no chaos when the limiter is not present. Because of the limiter the behavior of the circuit is independent of wave form, so that square waves give the same result as the sine waves used in the FM study. The results for BPSK are only preliminary and indicate that there are regions of the operating parameter ranges which require further investigation (Section 3.8 contains the details of this work).

2.1.3 Network Synchronization

Due to the importance of the synchronization of oscillators in the design of microwave systems, in electrical power generation, Josephson junction arrays, networks of clocks or computers distributed geographically, etc. preliminary work was begun on the synchronization to a common frequency of systems made up of many coupled digital phase locked loops (DPLL's). We studied the transition to the locked state in several different configurations and when the center frequencies are identical for all loops, and when they differ. A closed form expression was found for the synchronization frequency when the communication be-

tween DPLLs is bi-directional. (see section 3.9).

We have observed the boundaries between synchronized and chaotic behavior for two or more coupled DPLLs. We have also shown that populations of non uniformly sampled digital phase locked loops synchronize with a common frequency over a range of parameters. We found that the transition to the synchronized state and the parameter range where it is stable depend on the configuration of the system, with the time to lock improving with the number of couplings for a fixed number of coupled devices. The time to lock increases linearly with number of coupled devices if the number of devices is small. The time to lock approaches a constant value for large number of devices.

As the transition to the locked state and the parameter range where synchronization hold depend on the configuration of the system, we plan to continue our numerical investigations of different configurations. We will study such questions as: What is the optimum configuration of the system? What are the advantages and disadvantages of DPLL's versus analog PLL's for network synchronization? We also plan to do an experimental study of the synchronization of DPLL's.

3.0 Individual Reports

3.1 Nonlinear Dynamics of Self-Synchronizing Systems

3.1.1 INTRODUCTION

A synchronizing system is one that locks the phase of an output signal (the receiver) to that of an input signal (the transmitter). Here the signals are represented as

$$V(t) = A \sin(\phi(t))$$

where $\phi(t)$ is the phase. A particular device that accomplishes this is a phase locked loop (PLL). Such devices have proved useful in a variety of communication applications, including modulation and demodulation, and noise reduction¹. A PLL can be either analog or digital (DPLL), both types being easy to realize and obeying equations that are convenient to analyze². In particular, the DPLL's have mapping representations that allow straightforward numerical investigation of their nonlinear properties, that is, dynamics far from the locked state^{3,4,5,6}.

In the usual synchronization system, the transmitter signal consists of a single carrier frequency and is represented by a sinusoidal signal at constant amplitude and phase. A phase locked loop in the receiver is then used to lock the receiver phase to that of the transmitter. Recently it has been shown⁷ that a dynamical system described by three differential equations, exhibiting chaos, can be used to transmit a signal to a subsystem also described by those equations in such a manner that the subsystem is synchronized with the primary chaotic system. This opens up an interesting new possibility in that the phase of a receiver can be locked to that of a transmitter even if the transmitted signal is chaotic, i.e., consisting of a continuous spectrum of carrier frequencies. Such synchronized systems may have applications to the problem of secure communications, offering a possible alternative to conventional spread spectrum systems.

A particularly simple DPLL is a first-order non uniformly sampling loop, which, as we shall discuss in paragraph 3.1.2, has a circle map representation. If we couple two such DPLL's together, the resulting dynamics can be far more complicated than that of a single loop because the loops can switch asynchronously, so that far from the locked state one

DPLL may change state more than once while the other is not changing state. Thus, unlike the usual coupled map lattices⁸, there is no explicit mapping representation for such coupled devices. In coupled map lattices, the dynamics of all elements are evolved at the same instant of time according to a given rule, which by definition, is described by mapping equations.

In the following sections, we describe the behavior of a coupled system consisting of two first-order DPLL's in which the output of the second loop serves as the input for the first loop, and vice-versa. For some regions of the parameter space, the usual properties associated with a single circle map persist, while for other parameters, the overall dynamics is more complicated. We then show how two coupled first-order DPLL's can be used to implement a transmitting system that generates a chaotic carrier signal, and how a third loop can be used as a receiving system that locks to the phase of the chaotic carrier. In paragraph 3.1.2 we derive the dynamics of a single loop, showing that the dynamics can be described by a simple one-dimensional circle map. Such maps are known to have a rich dynamical behavior⁹, including quasiperiodic motion, regions of phase-locking, period-doubling to chaos and intermittency. Coupling two such DPLL's together such that the output of each loop is the input for the other loop, we obtain the algorithm for iterating the coupled system and obtain explicit mapping equations valid for some regimes. In paragraph 3.1.5 we analyze the dynamics of the two-coupled-loop system in detail and obtain numerically the conditions for the coupled chaotic motion. In paragraph 3.1.6 we introduce the receiving element and demonstrate phase locking of the receiver to the chaotic transmitted signal. We also study the effect of variation of the receiving loop parameters on the phase locking. The embodiment here has a particular simplicity that makes the concept of chaotic synchronization both transparent and potentially useful. In paragraph 3.1.6 we summarize our results and describe some extensions of the concept.

3.1.2 SYSTEM DESCRIPTION

A block diagram of a single, first-order, non uniformly sampling DPLL is shown in FIGURE 6.. It consists of a sample-and-hold (SH) and a variable frequency oscillator (VFO). During the operation, the SH takes a discrete sample $s(t_k)$ of the incoming signal at a sampling time t_k when the VFO signals it to do so at a positive going zero crossing. The sam-

ple is used to control the frequency of the VFO according to a given function $\omega(s)$ in such a way as to decrease the phase difference between the incoming signal and the oscillator output. As a result, there is a possibility of locked behavior when the oscillator frequency adjusts itself to the input frequency and locks to its phase, hence sampling always at the same point on the input signal.

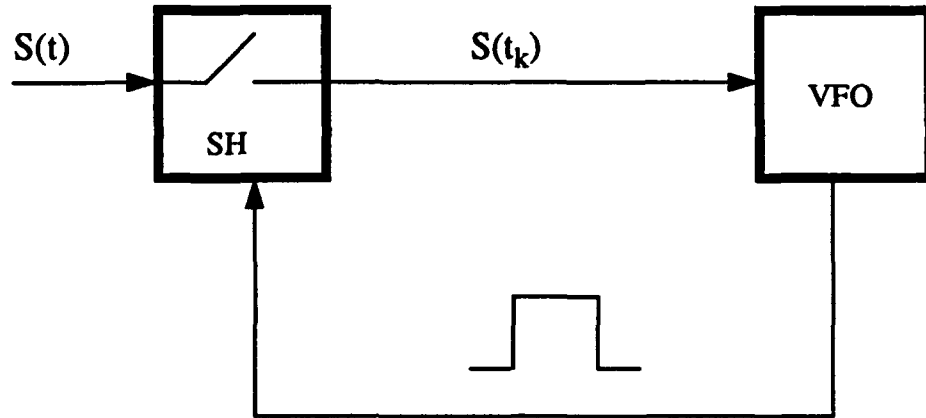


FIGURE 6. schematic representation of a single DPLL

Consider the case in which the incoming signal is given by.

$$s(t) = A \sin(\omega t + \theta_0)$$

Suppose that the period of the oscillator is linearly related to $s(t_k)$ as

$$T_{k+1} = T_0 + b s(t_k) \quad (1)$$

where $T_0 = 2\pi/\omega_0$. The center frequency ω_0 is the frequency of the VFO in the absence of the applied signal. It was shown by Gil and Gupta³ that in a loop governed by Eq. (1), the evolution of the phase difference between signal and oscillator output is described by the nonlinear difference equation

$$\phi(t_{k+1}) = \phi(t_k) - \omega b A \sin(\phi(t_k)) + 2\pi(\omega/\omega_0) \quad (2)$$

Eq(2) is the well known sine-circle map, which has been studied in detail as a prototype for the quasi-periodic route to chaos⁹. In the context of DPLL's, Eq(2) was studied by several authors⁴ after Gil and Gupta.

In normal practical devices, where the frequency, not the period, is linearly related to the input sample as

$$\omega(t_{k+1}) = \omega_0 + bs(t_k) \quad (3)$$

then another map is obtained for the phase difference:

$$\phi(t_{k+1}) = \phi(t_k) + \frac{2\pi\omega}{\omega_0 + basin\phi(t_k)} \quad (4)$$

This is also of the form of a circle map, and displays the usual behavior associated with such maps⁵.

3.1.3 Coupled Loops

The self-synchronization system of two coupled DPLL's, for which the forcing input in one loop is the oscillator output of the other loop, is shown in FIGURE 7.. We study here only the case in which the frequency of the oscillator is linearly related to the input sample according to Eq(3). Preliminary calculations show that if the coupled system is governed by Eq(1), similar qualitative results are obtained.

In we show a diagram that exemplifies the dynamics of the coupled system. The signals in the figure, which are taken to be sinusoidal, represent the time varying output of the VFO's. Each time that one of these signals crosses the t axis with a positive slope, the oscillator sends a signal to the SH and an input sample is taken from the VFO output of the other loop. The loop that samples switches its frequency to a new value according to Eq (3).

The evolution of the system follows the steps described by the following algorithm:

Given the frequencies ω_1, ω_2 and the phases θ_1, θ_2 of the two VFO's at $t=0$, then:

0) Initialization: Find what should have been the last sampling time t_i and the next sampling time t'_i for both loops $i=1,2$

$$t_i = \frac{\theta_i}{\omega_i} \quad (5)$$

$$t'_i = \frac{2\pi - \theta_i}{\omega_i} \quad (6)$$

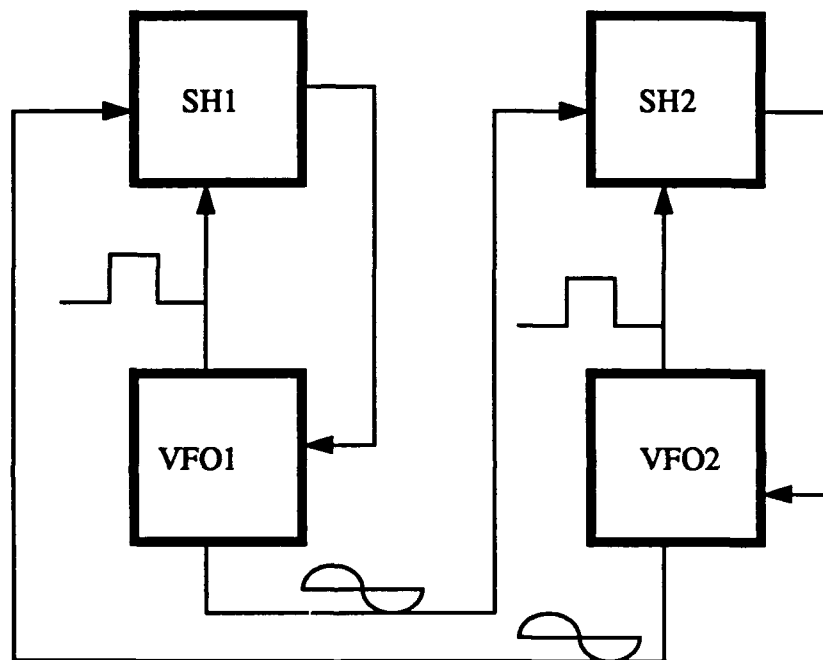


FIGURE 7. Two coupled self-synchronizing DPLLs

1) Search over the two DPLL's to find the loop "1" with the smallest time for the next sampling; that is, find "1" such that

$$t_i = \min(t'_i) \quad (7)$$

i=1,2.

2) Calculate the input sample value, which is taken from the output signal of the other VFO:

$$s_i(t'_1) = A \sin \phi_i \quad (8)$$

$$i \neq 1$$

where

$$\phi_i = \omega_i(t'_i - t_i) \quad (9)$$

3) Update the frequency of the loop "1" according to Eq(3):

$$\omega'_i = \omega_0 + b_1 s_i(t'_1) \quad (10)$$

4) Set

$$t_1 = t'_1$$

$$t'_1 = t_1 + 2\pi\omega'_1$$

Return to step 1.

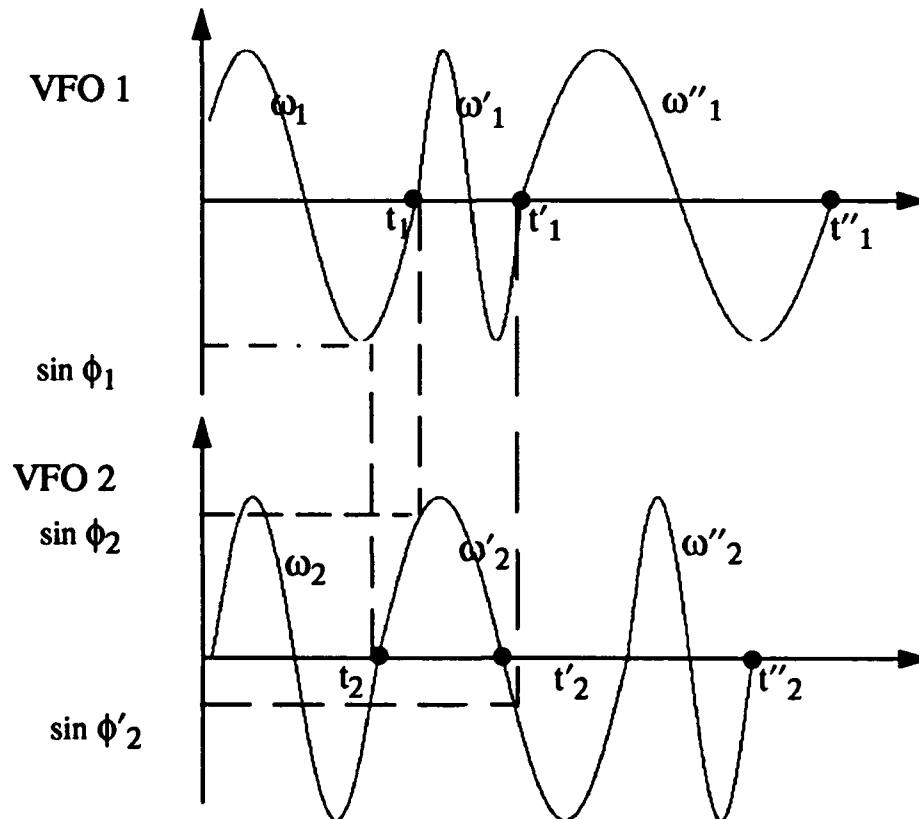


FIGURE 8. Schematic representation of the dynamics of the two coupled DPLLs

For any time t , the system state is determined by four variables, that is, the frequencies and the phases of the two loops. However, observe that the system state changes only at the sampling instants, $\phi_1=0 \bmod 2\pi$ or $\phi_2=0 \bmod 2\pi$. At these instants we need to know only the two variables ω and ϕ of the loop that does not sample. This is because

$$\begin{aligned}\phi &= 0 \\ \omega &= \omega_0 + bs(t_k)\end{aligned}$$

for the loop that samples. In this way, we can evolve the system at discrete times in a reduced variable space. For a surface of section, say $\phi_2=0$, and because

$$\omega_2 = \omega_1 \frac{\omega_1}{\phi_1}$$

the dynamics can be visualized in a two dimensional subspace ω_1, ϕ_1 . The evolution is therefore determined by three variables, (say ϕ_2, ω_1 and ϕ_1 , rather than the four variables of the total phase space. We note that we do not have an explicit mapping, as in the case of a single loop. The system evolution is instead described by the algorithm given above. We find that two equations for the phases govern the dynamics of the coupled system, namely

$$\phi_{i'} = \phi_i + 2\pi \frac{\omega_0 + b_i \sin \phi_j}{\omega_0 + b_j \sin \phi_i} \quad (11)$$

$$\text{or } \phi_{i'} = 2\pi + (-\phi_j) \frac{\omega_0 + b_i \sin \phi_j}{\omega_0 + b_j \sin \phi_i} \quad (12)$$

where i, j refers to the index of the loop, 1 or 2. The phases that appear on the right hand side of eqs. (11) and (12) are the phases associated with the last sampling times of loops i and j , and the primes refer to the next sampling time. The first equation applies when one loop samples at two or more consecutive times while the other loop does not sample. The second equation applies when successive sampling times originate from alternate loops. Note that we have taken $A=1$ since it appears always multiplied by the gain b and we can take this product as an unique parameter. Also, we consider that

the b 's are in principle distinct for the two loops, whereas the center frequencies ω_0 's are the same for both. This is done to reduce the dimensionality of the parameter space.

When we evolve the dynamics we do not know in principle the sequence in which Eqs. (11) and (12) will be applied; this will depend on the loop parameters. In a general situation we have to follow the steps of the algorithm described previously.

3.1.4 RESULTS

We numerically explored the dynamics of the two coupled DPLL system, described above, by varying the parameters ω_0 , b_1 and b_2 . Initially we considered two identical loops, i.e., same values for their parameters. In this situation we expected that we would not lose any important aspects of the dynamical behavior by observing the dynamics of only one of the loops. We therefore studied the behavior of one loop at the sampling times of the other, that is, we studied the system at the surface of section $\phi_i=0$, where i is chosen to be 1 or 2. Without loss of generality, we took $\omega_0=1$.

In FIGURE 9.a we show the steady state bifurcation diagram (after the transient period has died out) for ϕ_1 at $\phi_2=0$ as a function of b where $b_1=b_2$ for $\omega_0=1$. The dynamics is characterized by periodic cycles and a chaotic regime, which is interwoven with periodic windows, as in many dissipative dynamical systems. Initially the system locks in a period one cycle. Then it bifurcates to a period two cycle where a 'splitting' bifurcation appears¹⁰. A splitting bifurcation is observed when multiple basins of attraction emerge; the initial condition determines which basin of attraction will be chosen by the system. The new stable attractors have the same periodicity as the attractors which become unstable. This phenomenon has interesting consequences for the synchronization of coupled DPLL's, as we shall see in paragraph 3.1.4. Following the splitting bifurcation, we observe a cascade of period doubling bifurcations and beyond this a chaotic regime. By varying the center frequency ω_0 , we observed a similar qualitative behavior in a reverse order. This can be understood in terms of the trajectory of passing through an Arnold tongue⁹ (region of phase locking) in the parameter space. For $b_1 \neq b_2$, we observe period doubling sequences in the parameter plane, and also more complicated bifurcation diagrams for certain choices of the parameters, such as the one shown in FIGURE 9. b

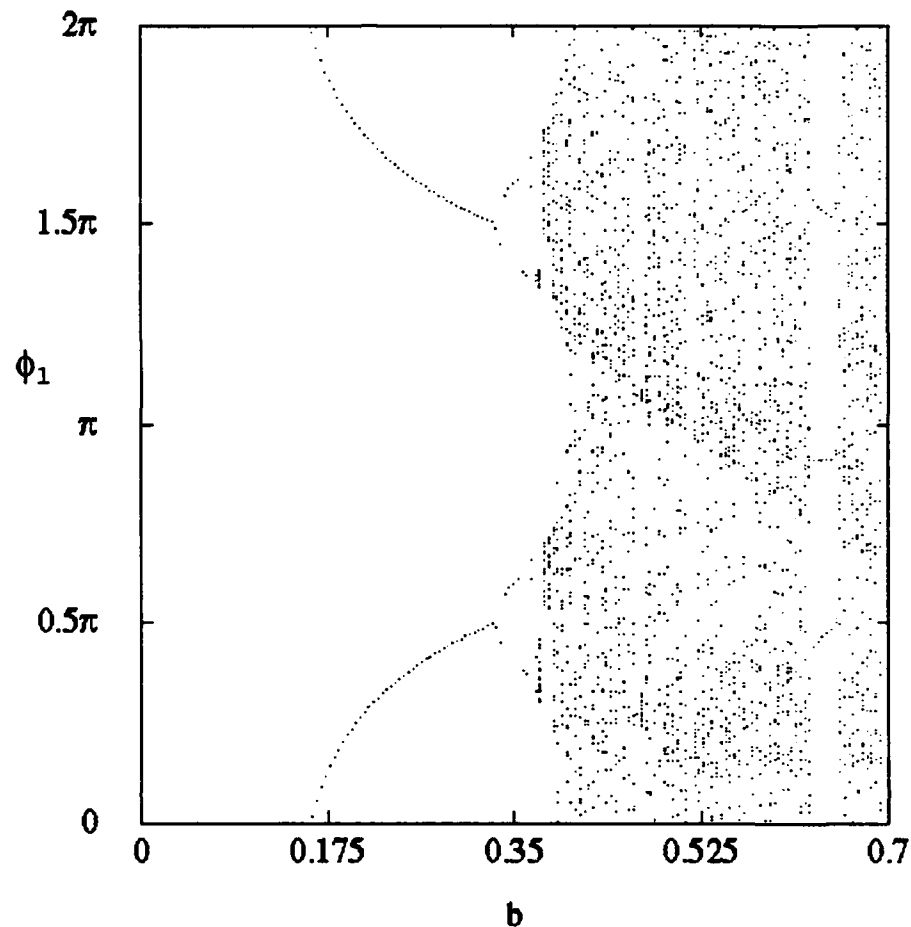


FIGURE 9.a Bifurcation diagram for the phase of loop 1 at $\phi_2 = 0$ as a function of $b \equiv b_1 = b_2$

The phase diagram in the b_1, b_2 plane for $\omega_0=1$ is shown in FIGURE 10. The black regions represent the parts of the parameter space with a very large period, which indicates that the system is chaotic at those points. As expected, the region of stability is mostly concentrated about the lower values of the parameter b . If one of the loops (or both) has b larger than a critical value ~ 0.35 , then phase diagram appears mainly chaotic. Some tongues of stability (periodic cycles) are observed after the entrance into chaos.

As stated previously, we did not know in principle the sequence in which Eqs. (11) and (12) would be applied. However, we observed numerically that anywhere within the period doubling sequence, in the steady state, the loops sampled in a fixed time sequence such that if one loop sampled twice, then the other loop also sampled twice, the first one then repeats the process, following exactly the sequence shown in

We observed this for several choices of the initial conditions and parameter values. We believe that this is a generic process in the bifurcation cascade.

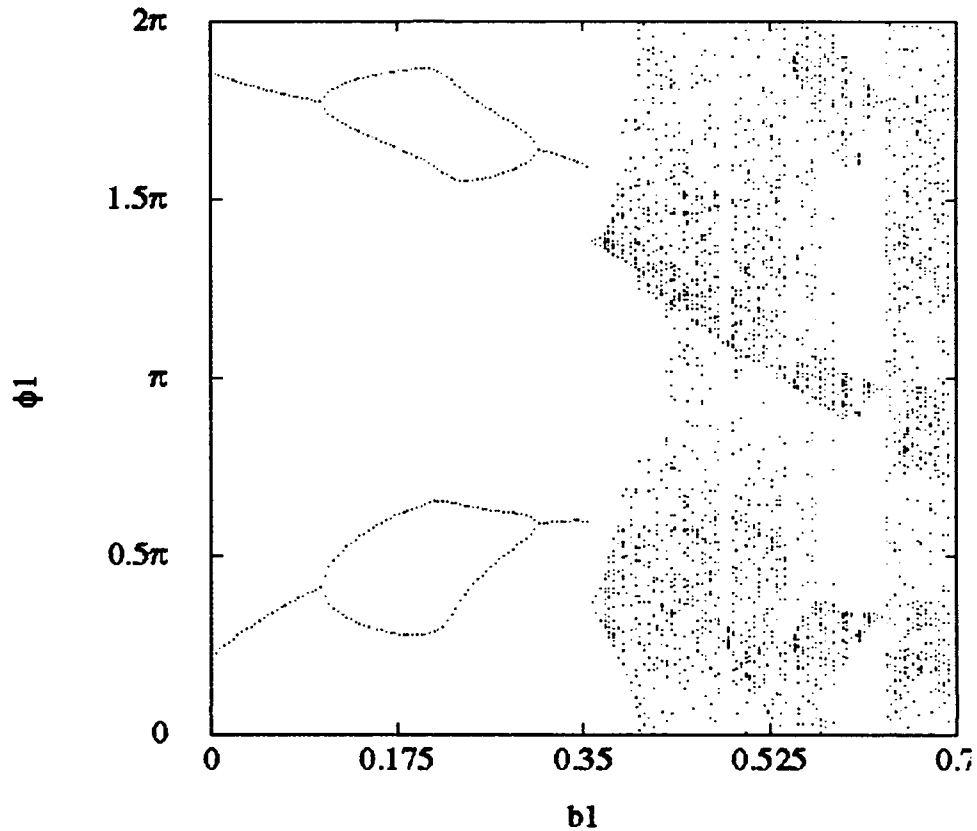


FIGURE 9. bBifurcation diagram for the phase of loop1 at $\phi_2 = 0$ as a function of b_1 for $b_2 = 0.35$ for $\omega_0 = 1$

For those parameter values for which the dynamics lies within the bifurcation sequence, we can write mapping equations to describe the evolution of the system. They are given by

$$\phi_{1'} = \phi_1 + 2\pi \frac{\omega_0 + b_1 \sin \phi_2}{\omega_0 + b_2 \sin \phi_1} \quad (13)$$

$$\phi_{2'} = 2\pi - \phi_{1'} \frac{\omega_0 + b_2 \sin \phi_{1'}}{\omega_0 + b_1 \sin \phi_2} \quad (14)$$

$$\phi_{2''} = \phi_{2'} + 2\pi \frac{\omega_0 + b_2 \sin \phi_{1'}}{\omega_0 + b_1 \sin \phi_{2'}} \quad (15)$$

$$\phi_{1''} = 2\pi - \phi_{2''} \frac{\omega_0 + b_1 \sin \phi_{2''}}{\omega_0 + b_2 \sin \phi_{1'}} \quad (16)$$

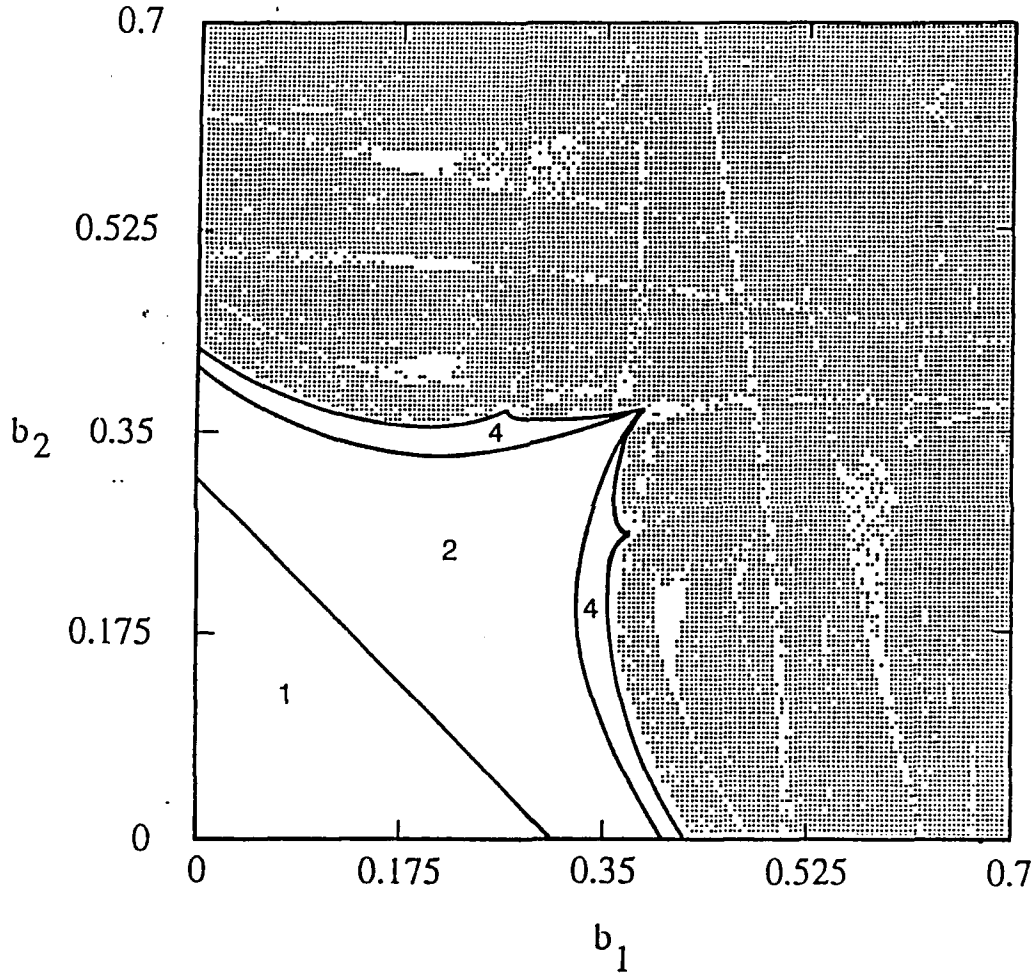


FIGURE 10. Phase diagram b_1 vs. b_2 for $\omega_0 = 1$, showing periodic orbits (labelled with the period) and chaotic regions (dotted)

where the double quotes refer to the second sampling. From the above equations one can calculate the Jacobian matrix for the transformation ϕ_i to $\phi_{i''}$. First we calculate the matrix that transforms ϕ_i to $\phi_{i'}$, and then multiply this matrix by the one that transforms $\phi_{i'}$ to $\phi_{i''}$. The trace of the resulting Jacobian matrix gives a measure of the stability of

the orbit. The most stable orbits have null trace, giving the parameter value that corresponds to the optimum stable system performance for a given cycle. We show in TABLE 2. the values of the parameter b (equivalent of $b_1 = b_2$) at these super stable orbits of the bifurcation cascade for $\omega_0=1$. Because of the splitting bifurcation, two super stable values are found for the 2-cycle. The sequence of b 's where the super stable cycles occur converges with a geometric ratio given by $\delta \sim 4.6692\dots$, as in quadratic mappings. Thus the two coupled DPLL's, when described by Eqs.(13),(14),(15),and(16) have the same universality class as dissipative systems governed by a quadratic map. At the period doubling bifurcations the trace of the Jacobian matrix is -1 , as expected; for the splitting bifurcation it is 1 .

TABLE 2. Values of $b \equiv b_1=b_2$ for the super stable orbits with $w_0=1$

Period	b
1	$\omega_0/2\pi$
2	0.2808560407
2	0.3496205907
4	0.3672296277
8	0.3715083345
16	0.3724198720
32	0.3726153586
64	0.3726572262

The border of stability of the period-one cycle can be obtained analytically by explicit examination of the Jacobian matrix near $\phi_1 = \phi_2 = 0$, which is the stable sampling phase of the 1 - cycle. Suppose that one perturbs the frequency of one loop in such a way that its frequency changes to $\omega_0 + \epsilon$; then one finds that at the next sampling time, the perturbation in the frequency with respect to the locked state will be

$$\epsilon' = \epsilon \left[1 - \frac{2\pi}{\omega_0} (b_1 + b_2) \right] \quad (17)$$

with the bracketed term being the trace of the Jacobian matrix. At the super stable cycle the perturbation vanishes, and therefore

$$b_1 + b_2 = \frac{\omega_0}{2\pi} \quad (18)$$

The period doubling bifurcation will occur when $\frac{\varepsilon'}{\varepsilon} = -1$.

Thus at this point,

$$b_1 + b_2 = \frac{\omega_0}{\pi} \quad (19)$$

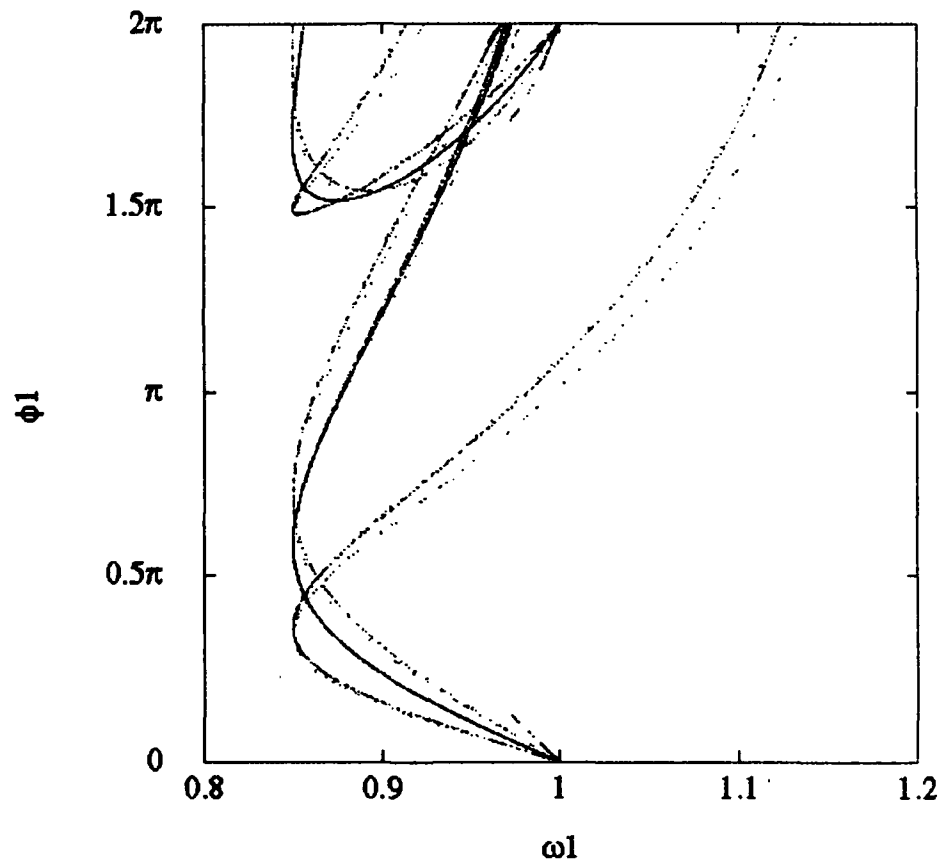


FIGURE 11. a Chaotic (or strange) attractor associated with loop 1 for $b_1 = 0.15$, $b_2 = 0.55$ and $\omega_0 = 1$ at $\phi_2 = 0$

We studied the chaotic regime in the phase vs. frequency plane, by taking a surface of section in which the phase of one (any one) loop is zero, as described previously. The behavior of the system can be characterized by Liapunov expo-

nents, which measure the mean rate of exponential separation of neighboring trajectories. The number of Liapunov exponents depends on the dimensionality of the system. If one of the exponents is positive, then the orbit is chaotic. We used the algorithm of ref. [11] to verify that the orbit at $b_1=0.15, b_2=0.55$ and $\omega_0=1$ has at least one positive Liapunov exponent and is therefore chaotic. In FIGURE 11. a we have used these parameters to plot the phase vs. frequency of loop 1 at $\phi_2=0$. A magnification of that figure (FIGURE 11b) shows a finely structured group of neighboring trajectories, which is a characteristic of strange attractors. Observe that for ϕ_1 near 0 the only possible value for ω_1 is $\sim \omega_0$. This is easily understood when we follow the dynamics shown in Every time that the phase of loop 1 is near 2π the input sample taken by loop 2 will be near zero. Consequently, the frequency of loop 2 will be close to ω_0 . The next loop to sample will be loop 1, and for an analogous reason its frequency will also be close to the center frequency.

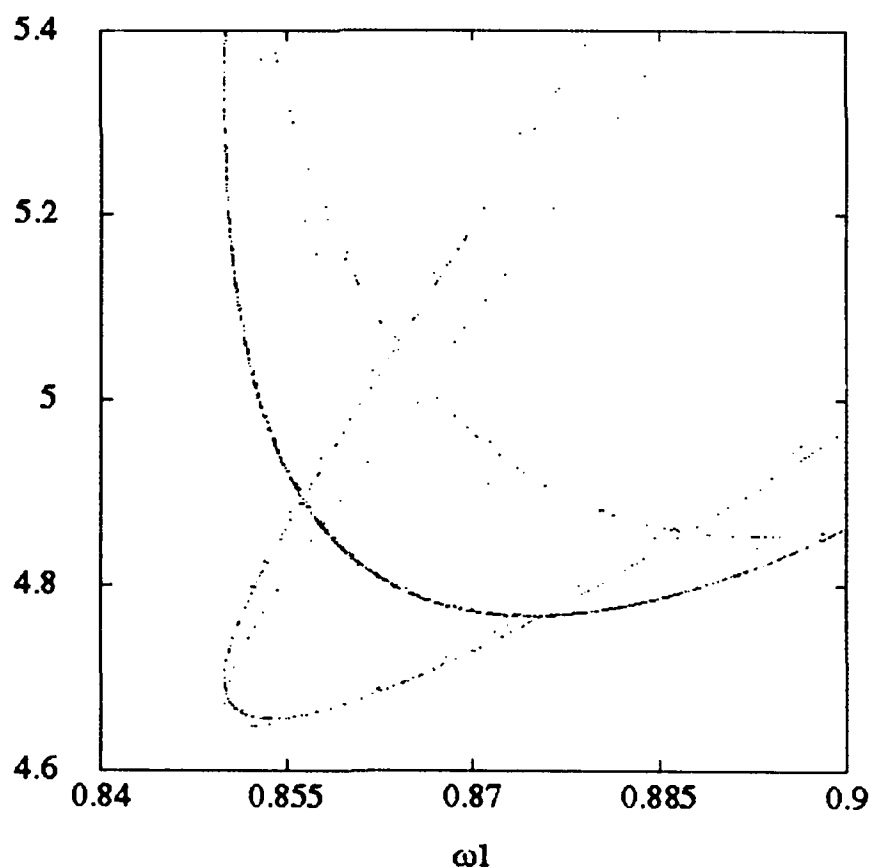


FIGURE 11b Magnification of box in figure 11a

3.1.5 SYNCHRONIZATION TO A CHAOTIC SIGNAL

We consider in this section the synchronization to a chaotic signal produced by the coupled DPLL's. The idea of synchronizing to chaotic signals was introduced recently by Pecora and Carroll⁷. They have shown that certain subsystems of nonlinear, chaotic systems can be made to synchronize by linking them with common signals. The synchronization is obtained from the influence of the chaotic driving system (the transmitter) on the response system (the receiver) while the driving system remain unperturbed. In their work, Pecora and Carroll investigated low-dimensional systems described by ODE's. They showed numerically that the necessary condition for the subsystem to follow the master system is that it have only negative Liapunov exponents. The concept of synchronized chaos was applied recently to spatially extended systems consisting of an array of coupled lasers¹². It was shown that there are extended systems where the synchronized chaos corresponds to spatial order and temporal disorder. By varying the external parameters this scenario breaks down and spatiotemporal chaos, or turbulence, may appear.

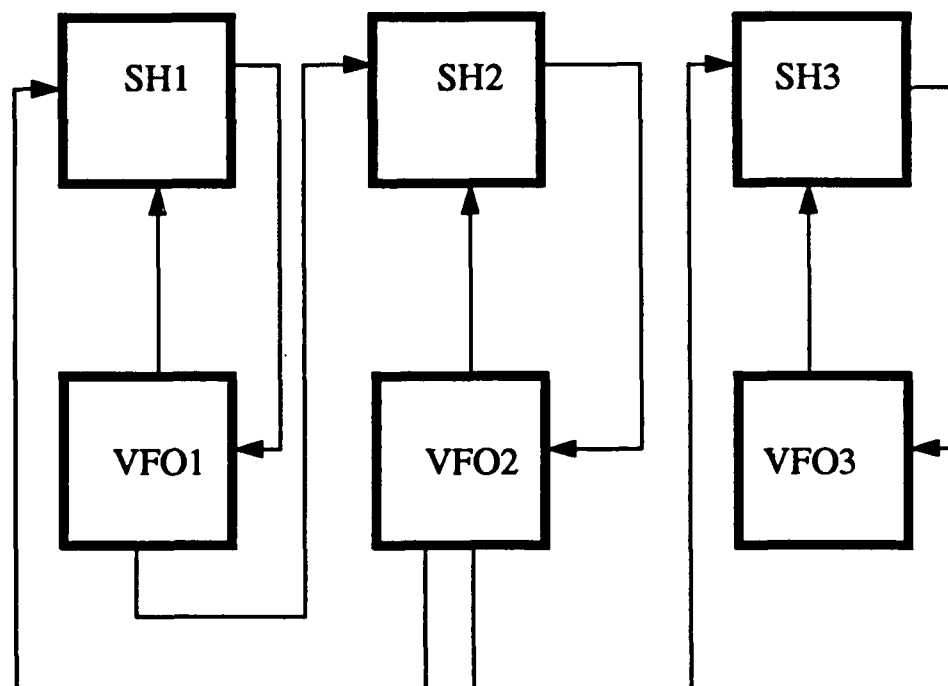


FIGURE 12. Communication system consisting of 3 DPLLs

The system we studied is shown in FIGURE 12.. The driving (or master) system is the two coupled DPLL system studied in the previous sections. The signal that originates from one of the VFO's (in this case the second one) is used to feed a slave system which consists of one single DPLL (the third loop). For the system shown, we investigated the parameter values that yield synchronization of the signals which originated from loop 1 and loop 3. We observe that there is a region of the parameter space where the slave system completely synchronizes to the driving system, whereas in other regions they seem practically uncorrelated. We showed in FIGURE 10. the region of the parameter space where chaotic behavior is expected for the driving system. If we pick the point $b_1=0.15$ and $b_2=0.55$ (for which we verified that the temporal dynamics is chaotic at the output of each VFO) we observe that at this point, for $b_3=b_1$, the steady state temporal evolution of the outputs of VFO 1 and VFO 3 are completely identical. This is illustrated in FIGURE 13., where we plot ϕ_3 against ϕ_1 , for the surface of section $\phi_2=0$. Thus, as in the case of coupled lasers¹², we observe a regime of temporal chaos and spatial order. The result here might have been expected because, as we can see from FIGURE 10., b_1 and b_3 are chosen such that loops 1 and 3 are operating in a regime that would be phase locked to an appropriate sinusoidal input signal. With a chaotic input, we cannot expect a phase locked output, but it is intuitive to expect that the stable loops will have identical outputs for identical inputs, as observed.

Those expectations are verified globally in FIGURE 14., in which the white region indicates the parameter region of synchronization. The necessary condition for the existence of synchronized chaos is that all the Liapunov exponents of the subsystem must be negative, as shown by Pecora and Carroll. We observe that the value $b_1=b_3 \leq 0.35$ roughly marks the border of synchronization. This corresponds approximately to the region of the parameter space, as seen in FIGURE 10., of regular motion for loop 1 and loop 3. Thus, even if loop 2 is chaotic, i.e., $b_2 \geq 0.35$ synchronization may be achieved between loop 1 and loop 3.

When $b_1=b_3 \geq 0.35$ (the cross-hatched portion), synchronization of loop 1 and loop 3 is not observed in most of the parameter space. This is consistent with their chaotic response to any input signal for these parameters. For this regime the resulting chaotic attractor appears to have a higher dimensionality (see FIGURE 15.), as in the case of the

array of coupled lasers¹². Contrast this figure with FIGURE 11. a, which shows a chaotic attractor in the region of synchronization. Theoretical questions remain concerning such problems as quantitative differences between different types of attractor, characterizing them by fractal dimension, etc.

For parameter values where multiple basins of attraction are found, the synchronization may not occur. One clear example in the figure is the region of the splitting bifurcations ($b_1 \sim b_2 \sim 0.33$). There we have two separate 2-cycles so that the system does not synchronize if loops 1 and 3 settle in different basins of attraction.

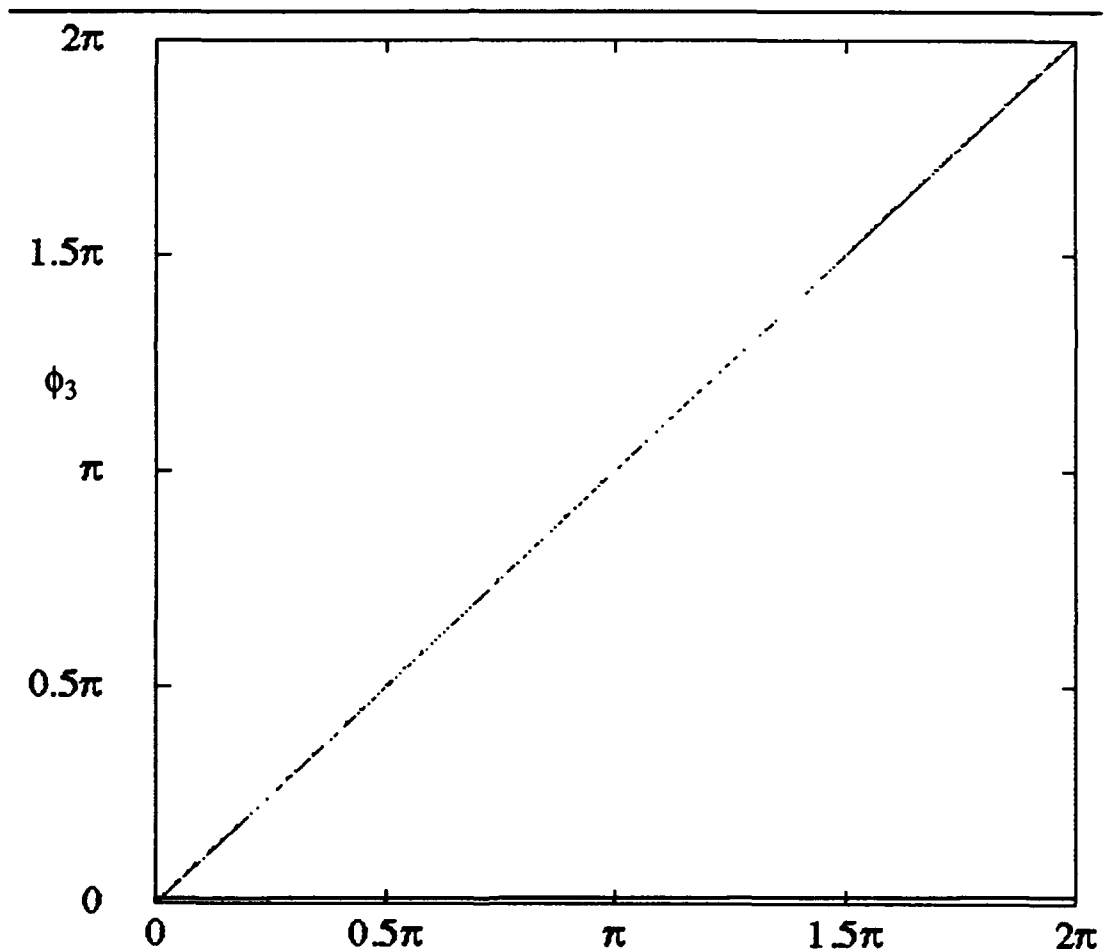


FIGURE 13. ϕ_1 vs. ϕ_3 for $\omega_0 = 1, b_1=b_3=0.15$ and $b_2=0.55$ at $\phi_2=0$

In a practical situation, it would not be possible to make b_1 and b_3 identical. Pecora and Carroll addressed this question for systems described by differential equations and found

that the synchronization persists, but with some error between the dynamical values of the master and slave system. We expect this same behavior in our coupled loop transmitter-receiver system, which indeed turns out to be the case. In FIGURE 16. we make $b_3=0.1$ and use the same values $b_1=0.15$ and $b_2=0.55$ given in FIGURE 13. We observe that in this case, when loop 3 is not completely identical to loop 1, the synchronization is degraded, but the loops have retained much of their correlation.

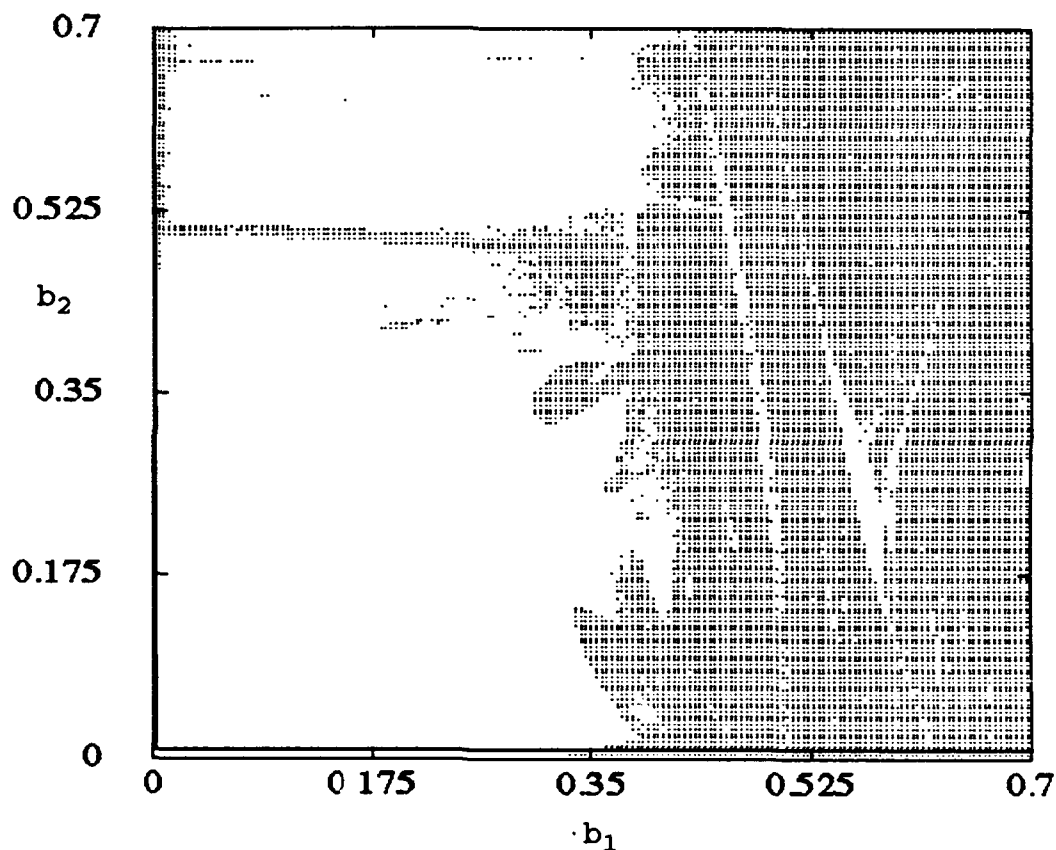


FIGURE 14. Diagram showing the region of synchronization (white region) for three DPLLs for $b_3 = b_1$

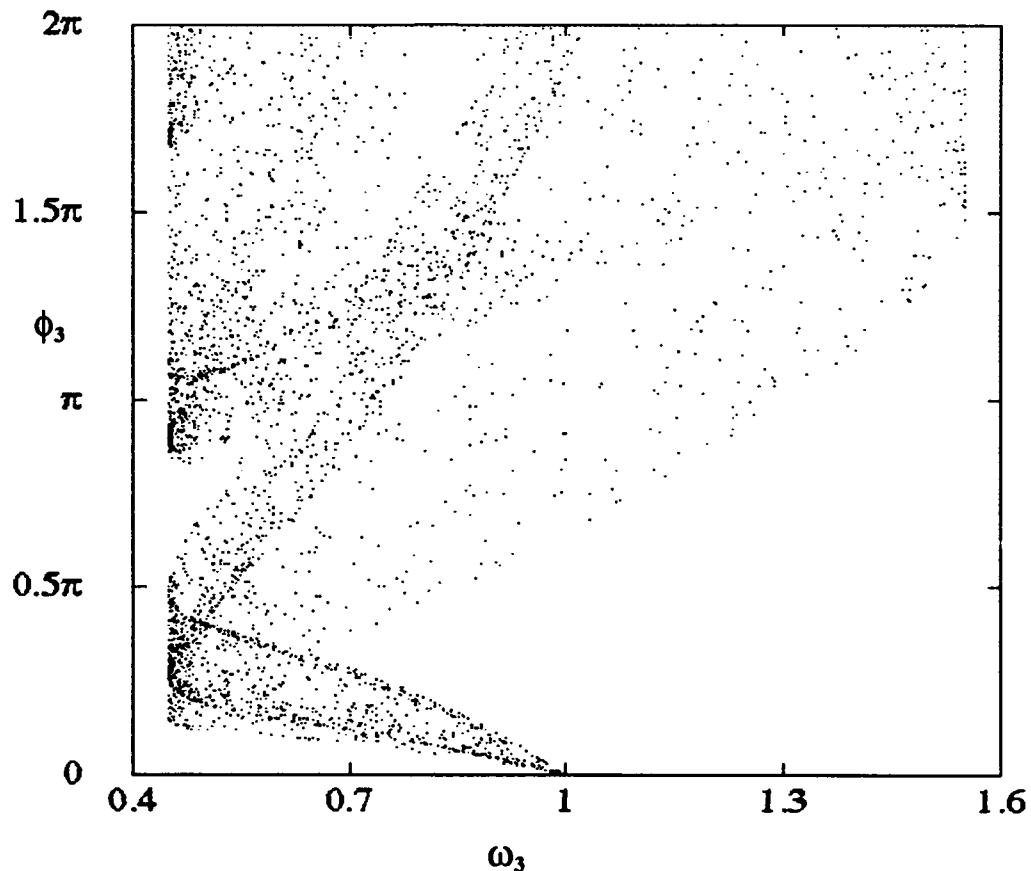


FIGURE 15. Chaotic attractor associated with loop 3 for $b_1 = b_2 = b_3 = 0.55$ and $\omega_0 = 1$ at $\phi_2 = 0$

3.1.6 CONCLUSIONS AND DISCUSSIONS

We have seen that a system of two coupled DPLL's has parameter ranges in which its behavior is one to one with its simpler relative, a single DPLL. The larger phase space allows more complicated behavior over other parameter ranges, and some of the similarities and differences are noted in our study. In particular, the sequence of bifurcations leading to chaos can be more complicated than period doubling, as seen in FIGURE 9.a. The chaos observed on the output of the two loops is different for the following two cases: (1) the b 's for both loops are chosen such that they are both unstable (see FIGURE 15.), and (2) one loop is stable and the other unstable (see FIGURE 11. a).

One key property of a coupled system that is of practical interest is that it can transmit a chaotic signal which can be

synchronized in time with a receiver. This synchronization to chaos, demonstrated in FIGURE 13., opens up new possibilities for communications systems. An exploration of the parameter range over which synchronization can be achieved (shown in FIGURE 14.) indicates general agreement with the intuitive notion that the identical subsystems of the transmitter and receiver must themselves be stable. If the subsystem parameters are not identical then the synchronization is not perfect, as shown in FIGURE 16. Information, however, can still be transmitted.

It is clear that our study represents only a beginning of a detailed exploration of both the nonlinear dynamics and the communications possibilities. Some practical questions concern methods of modulation and implementation. Quantification of synchronization degradation, shown qualitatively in FIGURE 16., is also important for practical applications.

A more general extension of this study concerns larger systems. It is clear from the above analysis that a repeater chain is more closely allied to the self-synchronizing system studied here than to a coupled map lattice with one way coupling (that it might superficially resemble). If the repeater is put on a circle, then it is also self-synchronizing. Studies of more complex interconnections also suggest themselves.

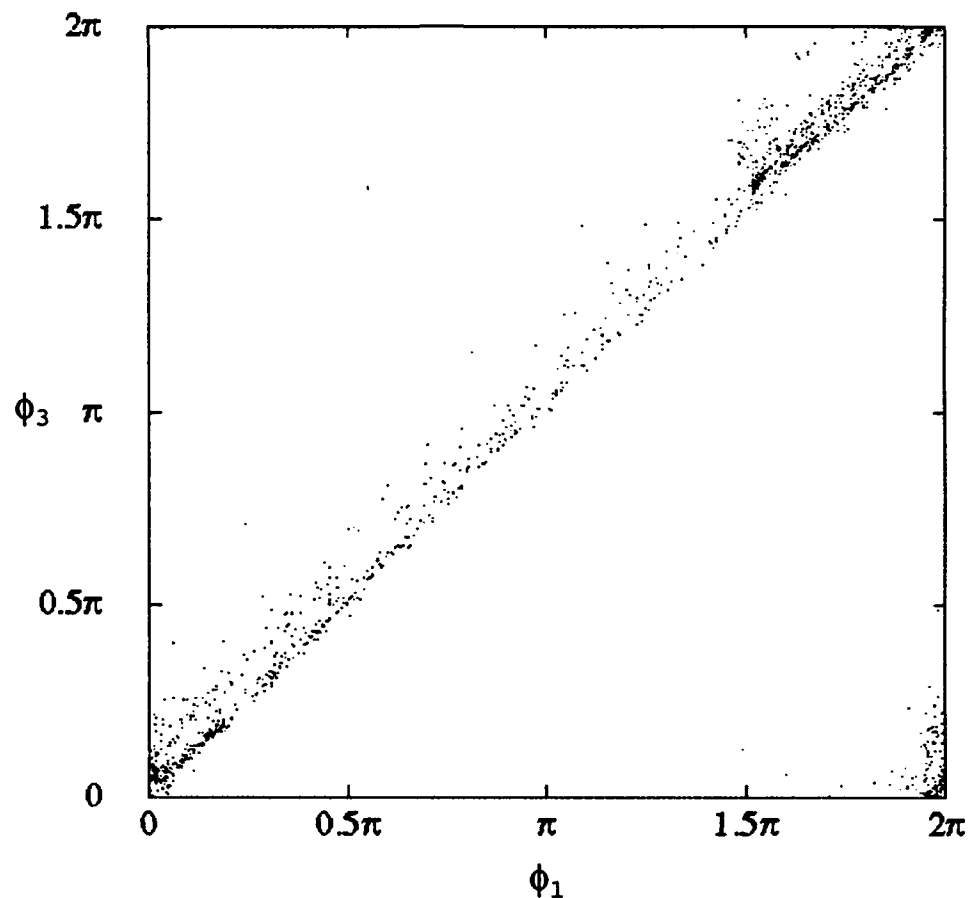


FIGURE 16. ϕ_1 vs. ϕ_3 for $\omega_0 = 1$ and $b_1 = 0.15$, $b_2 = 0.55$, $b_3 = 0.1$ at $\phi_2 = 0$

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3.2 SECURE COMMUNICATIONS BY SYNCHRONIZATION TO A CHAOTIC SIGNAL.

3.2.1 INTRODUCTION

The concept of synchronized chaos was introduced recently by Pecora and Carroll¹. They showed how two systems linked by a chaotic signal synchronize with each other. One potential application of this concept is to the problem of secure communications. The idea is to have two remote systems linked by the same chaotic signal and synchronized with each other. In section 3.1 this possibility was explored numerically in a system of coupled Digital Phase Locked Loops (DPLL's). Using two coupled loops as a transmitter of a chaotic signal, we showed how a third loop can synchronize with one of the transmitter elements.

Analog and digital PLL's are electronic devices used in a variety of communication applications such as modulation and demodulation, noise reduction, etc.², and also as synchronization devices to lock the phase of a receiver to that of a transmitter. In a single DPLL the phase difference between transmitter and receiver is described by a circle map when the input is a sinusoidal signal with a constant amplitude and frequency^{3,4}. Circle maps have been studied extensively in the past. They exhibit periodic cycles, quasiperiodic behavior and chaos⁵. For two coupled DPLL's we also observed a complicated behavior characterized by periodicity, quasiperiodicity and chaos. The work reported here is a more extensive study of self-synchronization of DPLL's and synchronization to a chaotic signal. The DPLL's considered here have different features from those studied in section 3.1, as they correspond more closely to the experimental system studied. This section is organized as follows: In section 3.2.2 we give a description of the system studied and present an algorithm to evolve the dynamics of coupled DPLL's. In section 3.2.3 we study in detail two coupled DPLL's. We investigate the synchronization to a chaotic signal using these two coupled DPLL's as a transmitter in section 3.2.4. In section 3.2.5 we study the quantification of the synchronization using the concept of mutual information. In section 3.2.6 we study the synchronization in more complex systems. The last section presents our conclusions.

3.2.2 SYSTEM DESCRIPTION

FIGURE 17. is the block diagram of a single, first-order, nonuniformly sampling DPLL, whose block diagram is shown in.

It consists of a sample-and-hold (SH) and a variable frequency oscillator (VFO). During the operation, the SH takes a discrete sample $v(t_i)$ of the incoming signal at the sampling time t_i when the VFO signals it to do so. The sample value v is used to control the frequency of the VFO according to a given function in such a way as to decrease the phase difference between the incoming signal and the oscillator output. As a result, for a range of parameters, there is a possibility of locked behavior when the oscillator frequency adjusts itself to the input frequency and locks to its phase, hence sampling always at the same point on the input signal.

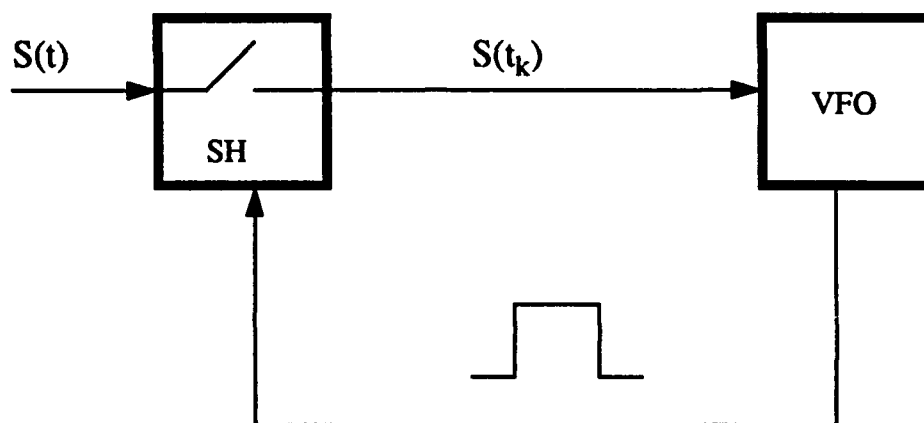


FIGURE 17. Schematic representation of a single DPLL

It is easily shown⁴ that when the input signal is a sinusoidal function and the frequency of the VFO is linearly related to the sampled value $v(t_i)$ as

$$f' = f^0 - b[v(t_i) + v^{\text{off}}] \quad (20)$$

that the phase difference between signal and the VFO output is described by a circle map. This kind of nonlinear map displays a rich phase space with tongues of periodic cycles, quasiperiodic behavior and chaos⁵. In eq. (20) f^0 is the center frequency of the VFO, i.e., its frequency in the absence of applied signal, b is the loop gain, and v^{off} is an offset voltage that may be added to the signal in order to bring it to the appropriate voltage range of operation in an

experimental device.

We can generalize this operation to a more complex configuration with N interconnected loops, each loop having a VFO output described by a wave form $v_j (j=1, \dots, N)$. In this system, every time that a v_j attains its peak value the j th loop takes a sample from the outputs of the VFO's to which it is connected. The input to the j -th loop is assumed to be given by a linear combination of the VFO outputs of the other loops, that is

$$s(t_i) = \sum_{j=1}^N a_{ij} [v_j \phi_j(t_i) + v_j^{\text{off}}] \quad (21)$$

The matrix $A=[a_{ij}]$ is called the interconnection matrix for the system. In our examples we consider $a_{ii}=0$. The value $s(t_i)$ is used to adjust the frequency of the i th VFO according to

$$f'_i = f_i^0 - b_i s \quad (22)$$

where f_i^0 and b_i are the center frequency and the gain, respectively, of the i th VFO. For a system of two coupled loops it is possible to derive mapping equations that describe the evolution of the system⁶. For more complex systems of coupled DPLL's it may be difficult or impossible to find such maps analytically. We can, however, easily evolve a system of any number of DPLL's in any configuration, using the algorithm presented in Ref. 5 and described below.

ALGORITHM: Suppose that in a system of N DPLL's interconnected through the matrix A the following information is given at $t=0$: the VFO's output waveforms v_i , the instantaneous frequencies functions f_i , the initial phases $\theta_i(0)$, then
0) Initialization: Find what should have been the last sampling time t_i and the next sampling time t'_i for each loop $i=1, \dots, N$

$$t_i = -\frac{\theta_i}{f_i} \quad (23a)$$

$$t'_i = \frac{1 - \theta_i}{f_i} \quad (23b)$$

1) Search over the DPLL's to find the loop 1 with the smallest time for the next sampling; that is, find 1 such that

$$\begin{aligned} t'_1 &= \min [t'_i] \\ i &= 1, \dots, N \end{aligned} \quad (24)$$

2) Calculate the input sample value, which is taken from the output signal of the other VFO's according to (21), taking

$$\phi_j(t_i) = f_j(t'_1 - t_j) \quad (25)$$

3) Update the frequency of the loop 1 according to eq. (22).
4) Set $t_1 = t'_1$ and $t' = t + 1/(f')$. Return to step 1.

3.2.3 TWO COUPLED LOOPS

In this section we study the dynamics of two coupled loops, where the input to one loop is the output of the other loop, and vice-versa as shown schematically in FIGURE 18. In the experimental device studied these outputs are voltages, which have a triangular wave form, and the sample is taken at the peak of the wave. We can use the convention that at this instant the phase of the wave is zero. Thus we represent the output signal of the VFO's as $v(t) = Ah(\phi(t))$ with

$$h(\phi(t)) = \begin{cases} -4\phi(t) + 1 & 0 \leq \phi(t) \leq \frac{1}{2} \\ 4\phi(t) + (-3) & \frac{1}{2} \leq \phi(t) \leq 1 \end{cases} \quad (26)$$

where $\phi(t) = ft$, with f the frequency, and $0 \leq t \leq 1/f$. In this coupled loop system each time that one of the triangular waves attains $\phi_i = 0 \pmod{1}$ the oscillator sends a signal to its SH which then samples the VFO output of the other loop. The loop that samples switches its frequency to a new value according to eq. (22). In FIGURE 19. we show a diagram that illustrates the algorithm given above for the two self-synchronized DPLL's, with a waveform given by eq. (26). The signals in the figure represent the time varying output voltages of the VFO's. The two main differences between this system and the one studied in section 3.1 are that here the wave is

triangular rather than sinusoidal and the sampling is taken at the peak of the wave rather than at a zero crossing, so that it corresponds to the experimental configuration. Some of the consequences due to this will be discussed in the next sections.

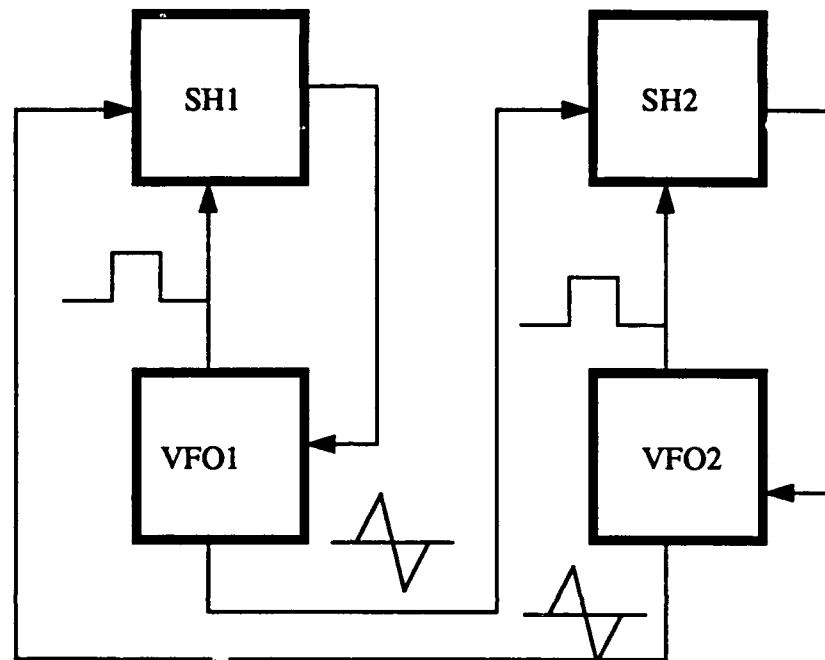


FIGURE 18. Two coupled self synchronizing DPLLs

In a system of two coupled DPLL's, for any time t , the system state is determined by four variables, that is, the frequencies and the phases of the two loops. However, the system state changes only at the sampling instants, $\phi_1=0 \pmod{1}$ or $\phi_2=0 \pmod{1}$. At these instants we need to know only the two variables (f and ϕ) of the loop that does not sample. This is because $\phi=0$ and $f=f^0-b_s(t_1)$ for the loop that samples. In this way, we can evolve the system at discrete times in a reduced variable space. For a surface of section, say $\phi_2=0$, and because $f_2=f_2(f_1/\phi_1)$, the dynamics can be visualized in a two dimensional subspace (f_1, ϕ_1) . The evolution is therefore determined by three variables, (say $\phi_2 \equiv 0$, f_1 and ϕ_1), rather than the four variables of the total phase space.

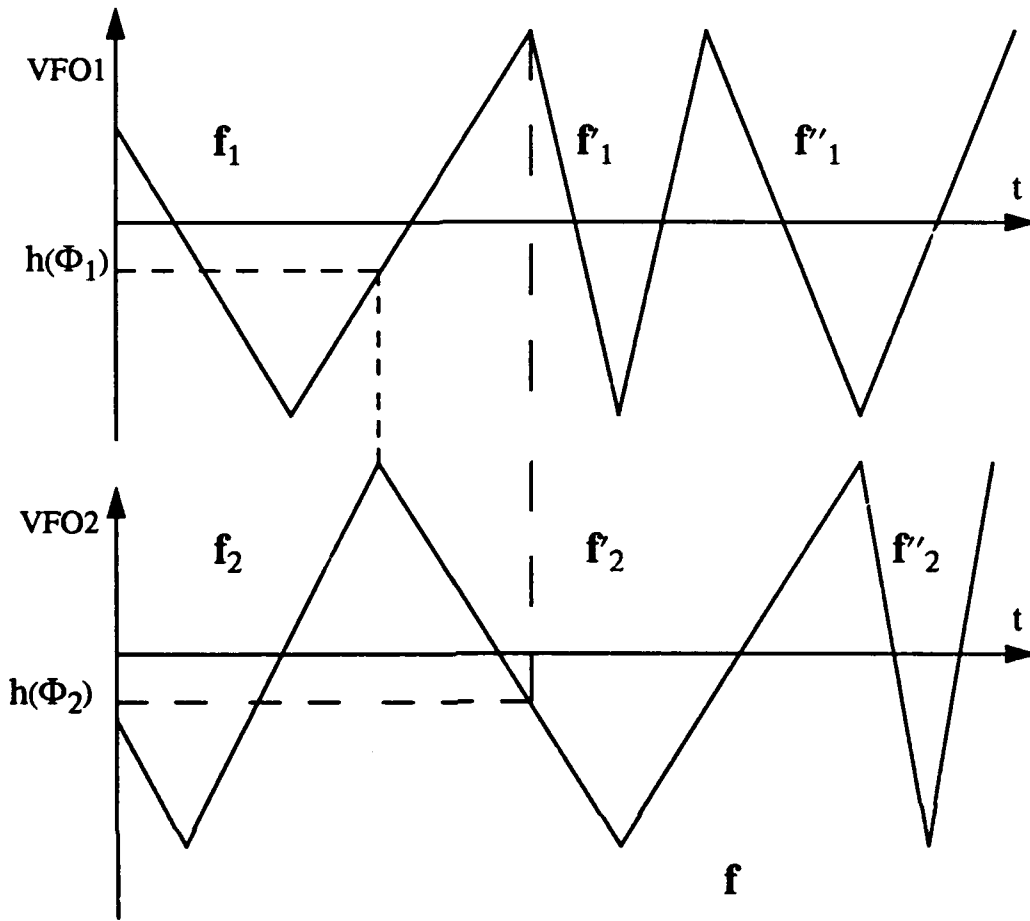


FIGURE 19. Schematic representation of the dynamics of the two coupled DPLLs

There are eight parameters in the coupled system. For each loop we have the amplitudes A_i 's, the gains b_i 's, the center frequencies f_i^0 's and the offset voltages v_i^{off} 's. We can normalize the parameters in the following way. The equations that determine the dynamical evolution of the loops are

$$f'_1 = f_1^0 - b_1 [A_1 h(\phi_2) + v_1^{\text{off}}], \phi_1 = 0 \quad (27a)$$

$$f'_2 = f_2^0 - b_2 [A_2 h(\phi_1) + v_2^{\text{off}}], \phi_2 = 0 \quad (27b)$$

Dividing Eq. (8) by $f_2^0 - b_2 v_2^{\text{off}}$ we obtain

$$\bar{f}_1' = f^0 - B_1 h(\phi_2) \quad (28a)$$

$$\bar{f}_2' = 1 - B_2 h(\phi_1) \quad (28b)$$

where

$$\bar{f}_1' = \frac{f_1'}{f_2^0 - b_2 v_2^{\text{off}}}, \quad f^0 = \frac{f_1^0 - b_1 v_1^{\text{off}}}{f_2^0 - b_2 v_2^{\text{off}}}, \quad B_i = \frac{b_i A_i}{f_2^0 - b_2 v_2^{\text{off}}} \quad (28c)$$

Thus there are three dimensionless fundamental parameters in the system, which are the two normalized gains B_1 and B_2 and the normalized center frequency f^0 of one of the two loops, say loop 1. Since the frequencies of these discrete time systems are positively defined, we must have from eqs. (28a), (28b), and (28c) that $B_1 < f^0$ and $B_2 < 1$, since $h(\phi) \in [-1, 1]$. By varying these three parameters we observe numerically in the system of two coupled loops, regular, quasiperiodic and chaotic behavior. We begin by doing an analytical analysis of the locked state, i.e., when both loops synchronize to a common frequency \bar{f}_s . In this case $\phi_1(\phi_2=0) = -\phi_2(\phi_1=0) \equiv \Delta\phi$. From eqs. (28a), (28b) and (28c) we obtain

$$\bar{f}_s' = f^0 - B_1 h(-\Delta\phi) \quad (29a)$$

$$\bar{f}_s' = 1 - B_2 h(\Delta\phi) \quad (29b)$$

By noting that $h(\phi)$ is an even function, we obtain from this system of equations:

$$\bar{f}_s' = \frac{B_2 f^0 - B_1}{B_2 - B_1} \quad (30a)$$

$$h(\Delta\phi) = \frac{1 - f^0}{B_2 - B_1} \quad (30b)$$

We see immediately that if $B_1=B_2$, f_s and $h(\Delta\phi)$ are undefined. No locked state exists. Also, if there is parameter matching between the two loops, i.e. $B_1=B_2$ and $f^0=1$, then any initial condition given to the system is marginally stable. Thus, in our numerical results we do not plot any solution when there is parameter matching between the loops. The situation would be different if $h(\phi)$ were an odd function, as was the case studied in section 3.1. There we obtained a stable locked state when all the parameters of the two loops were identical. The loops will be in phase when $\Delta\phi=0$, which implies $h(\Delta\phi)=1$. From eq. (30b) one sees for this case that the relation $f^0=1+B_1-B_2$ must be satisfied. If $f^0=1$ we obtain $\bar{f}_s=1$ and $h(\Delta\phi)=0$, which implies $\Delta\phi=0.25$ or $\Delta\phi=0.75$. We observe numerically that if $B_1<B_2$ ($B_1>B_2$) then $\Delta\phi=0.75$ ($\Delta\phi=0.25$) are unstable solutions.

We show in FIGURE 20., FIGURE 21. a and FIGURE 21. b bifurcation diagrams for two typical cases. In FIGURE 20. we plot ϕ_1 vs. B_1 at $\phi_2=0$ for fixed values of B_2 and f^0 , namely, $B_2=0.2$ and $f^0=1$. Observe that at $B_1=B_2$ there is a jump in $\Delta\phi \equiv \phi_1$ for the locked state solution, as discussed in the previous paragraph. Next we take $B_1=B_2=0.2$ and plot ϕ_1 vs. f^0 at $\phi_2=0$ (FIGURE 21. a) and ϕ_2 vs. f^0 at $\phi_1=0$ (FIGURE 21. b). In the last example no locked state exists, i.e., a state where both loops would have the same frequency, as obtained from eqs. (30a) and (30b),. The big window around $f^0=2$ corresponds to the case $\bar{f}_2=2\bar{f}_1$. The complete phase diagram is situated in a three dimensional space, since we have three fundamental parameters. We study some particular planes of the phase diagram. In the first case we take $B_1=0$. This corresponds to the case in which the coupling between loops is only in one direction. That is, the input of loop 2 is a triangular wave with constant frequency f^0 . Similarly to what was done in Ref. [5], we can easily derive that the phase difference between loops 1 and 2 at the sampling instants of loop 2 is given by

$$\phi'_1 = \phi_1 + \frac{f^0}{1 - B_2 h(\phi_1)} \quad (31)$$

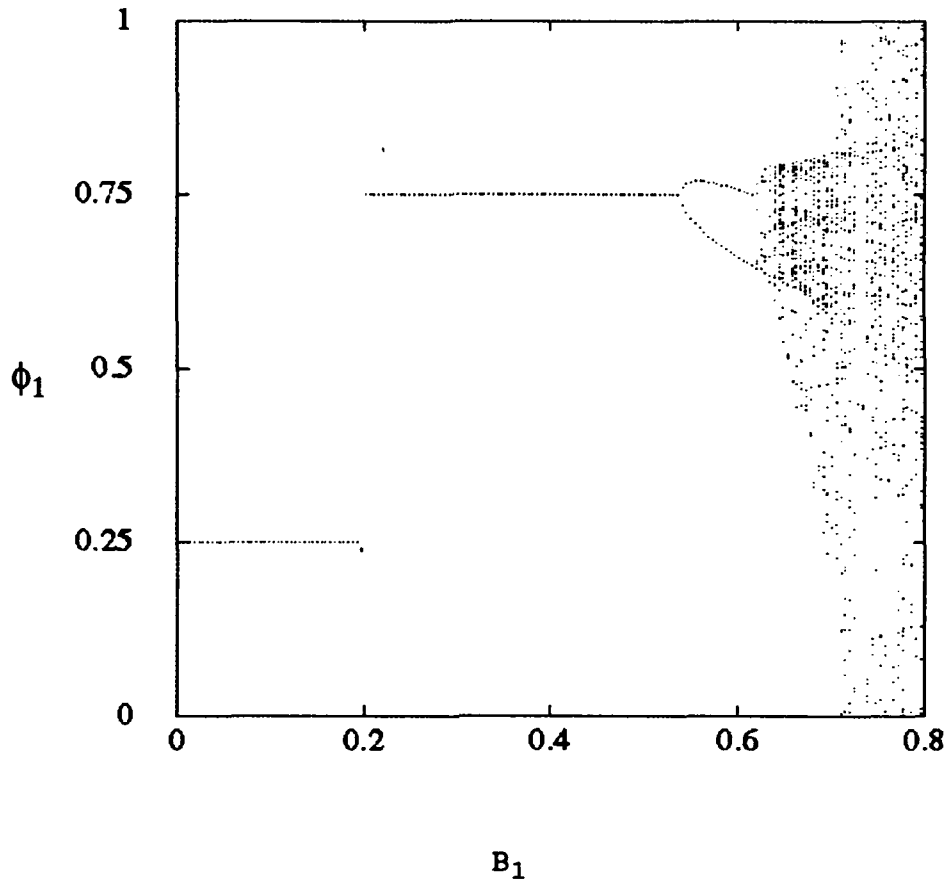


FIGURE 20. Bifurcation diagram for ϕ_1 ($\phi_2=0$) as a function of B_1 for $B_2=-2$ and $f_1^0 = 0$

where $h(\phi_1)$ is given by eq. (26). This is a one-dimensional nonlinear map which shares some properties with circle maps. Because of the discontinuity in the $h(\phi)$ derivative this map has a phase diagram that is topologically different from the diagram of the circle map. In FIGURE 22. we show that phase diagram of the map (eq (31)). The black regions were determined numerically to have positive Liapunov exponent λ . The Liapunov exponent measures the rate of the exponential separation between two neighboring trajectories, and it is defined as⁷

$$\lambda = \frac{\left[\lim_{N \rightarrow \infty} \sum_{n=1}^N \log \left| \left(\frac{d}{d\phi_1} \phi'_1 \right)^n \right| \right]}{N-1} \quad (32)$$

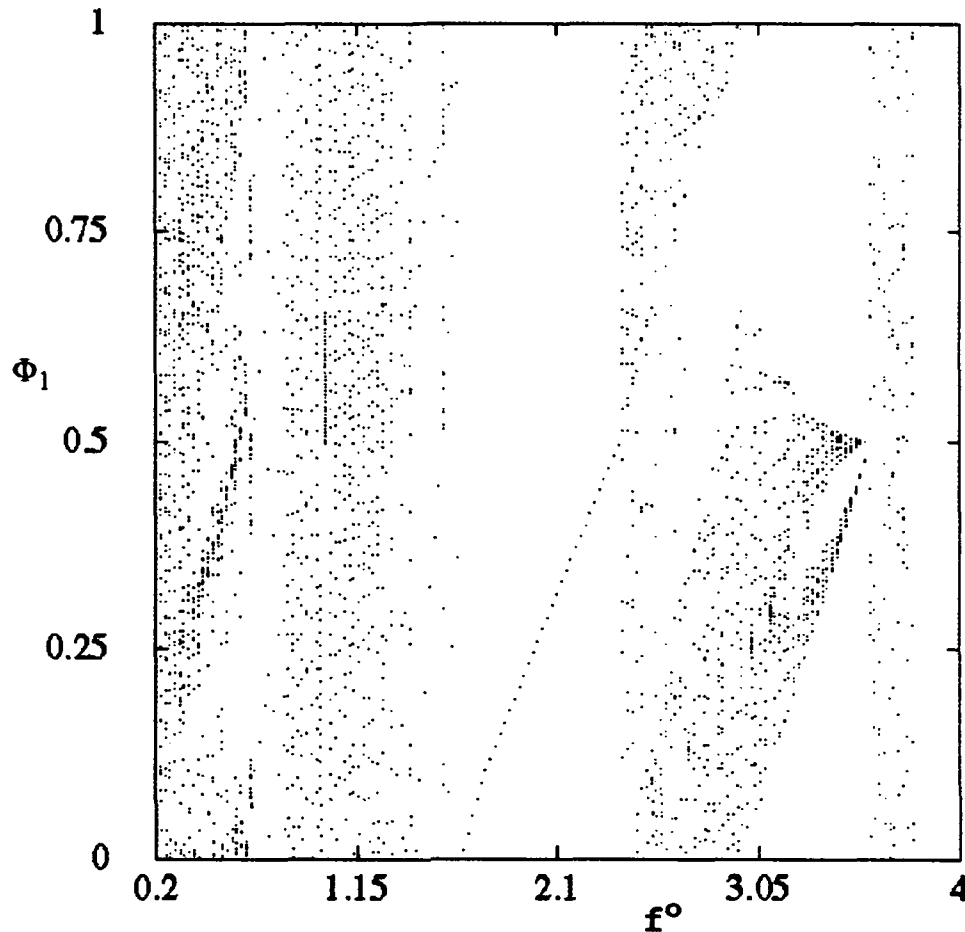


FIGURE 21. a Bifurcation diagram for $\phi_1(\phi_2 = 0)$ versus f^0 with $B_1 = B_2 = .2$

where the superscript n denotes the iteration index. It is well known that if a system has at least one positive Liapunov exponent in a given region of the parameter space, then the system is chaotic in that region. We considered λ positive in the calculations when $\lambda > 10^{-3}$ for 30,000 iterations after a transient of 3000 iterations. In the region where chaotic motion can appear the map is noninvertible. The border of invertibility of (eq (31)) is shown in Fig. (6) by a dashed line and is determined by $f^0 = (1 - B_2)^2 / (4B_2)$. We observe the existence of tongues of stability similar to the Arnold tongues. However, as we mentioned, this phase diagram is not topologically identical to the phase diagram of a circle map. For instance, at $f^0 = 1$ a circle map would display a sequence of period doubling bifurcations, which is not observed here. The bifurcation sequence in our map is truncated at the 2-cycle.

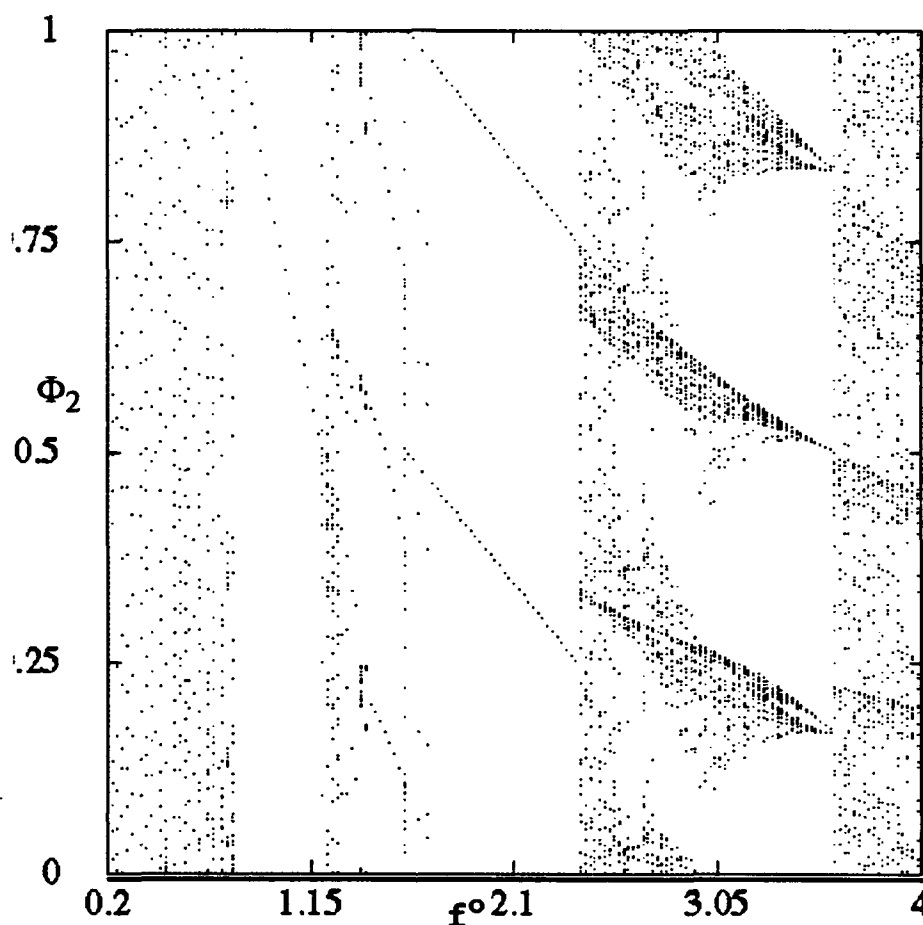


FIGURE 21.b Bifurcation diagram for ϕ_2 ($\phi_1 = 0$) versus f° with $B_1 = B_2 = .2$

We study two simplified cases of the coupled system. First we study the plane $B \equiv B_1 = B_2$. Now we have coupling in both directions. In this case the calculation of the Liapunov exponent is not straightforward, because of the discontinuities in the mapping equations⁶. We applied some tests and algorithms used generally for experimental series⁸ to calculate the Liapunov exponent. We show in FIGURE 23.a the phase diagram for the plane B vs. f° . The white region indicates periodic motion, and the shaded part indicates a very large period, which implies either quasi-periodicity or chaos. We consider the motion periodic if $|\phi_1^{1000} - \phi_1^1| \leq 10^{-6}$ where the superscript indicates the iteration number of loop 2. A transient of 30,000 iterations was used. We expect that the quasiperiodic behavior in analogy with the map given by eq (31), is represented by the dots seen in the region where B is small. For large B , where we have most of the shaded region, we made several tests using the algorithm given in Ref. 8 to

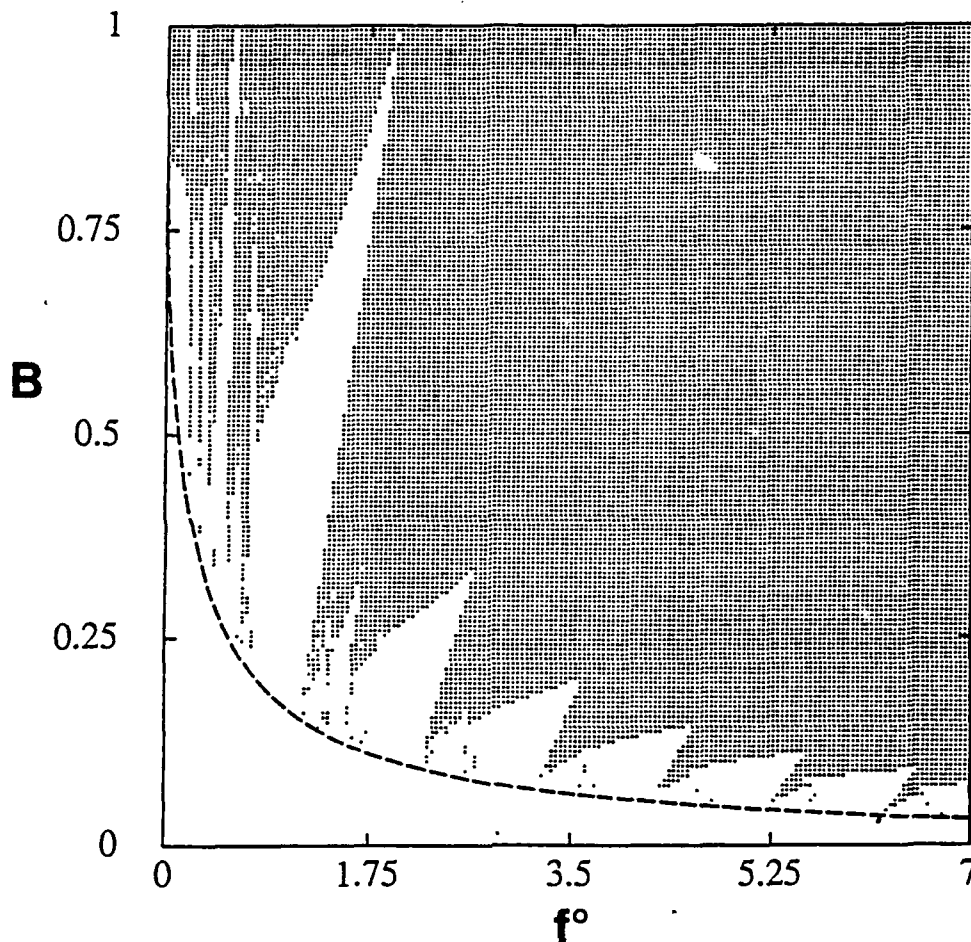


FIGURE 22. Phase diagram associated with equation 31 showing the chaotic region (dotted) and periodic and quasiperiodic solutions (white). The border of invertibility is indicated by a dashed line.

confirm that the Liapunov exponent there is positive. Now we consider $f^0=1$ and plot in FIGURE 23. b (shaded) the regions in the B_2 vs. B_1 plane where the motion is nonperiodic, according to the criterion used to make FIGURE 23.a. The stable, non-chaotic, regime is most concentrated around the line $B_1=B_2$, and the diagram is symmetric with respect to this line.

3.2.4 SYNCHRONIZATION TO A CHAOTIC SIGNAL}

We consider in this section the synchronization to a chaotic signal produced by the coupled DPLLs using an idea introduced recently by Pecora and Carroll¹. They have shown that certain subsystems of nonlinear, chaotic systems can be made to synchronize by linking them with common signals. The synchronization is obtained by transmitting a variable of the

chaotic driving system (the transmitter) to be a corresponding variable of the response system (the receiver) while the driving system remain unperturbed. In their work, Pecora and Carroll investigated low-dimensional systems described by ODEs. They showed numerically that the necessary condition for the subsystem to follow the master system is that it have only negative Liapunov exponents. We have shown in section 3.1 that this concept can be applied to coupled DPLLs. The concept of synchronized chaos was applied recently to spatially extended systems consisting of an array of coupled lasers⁹.

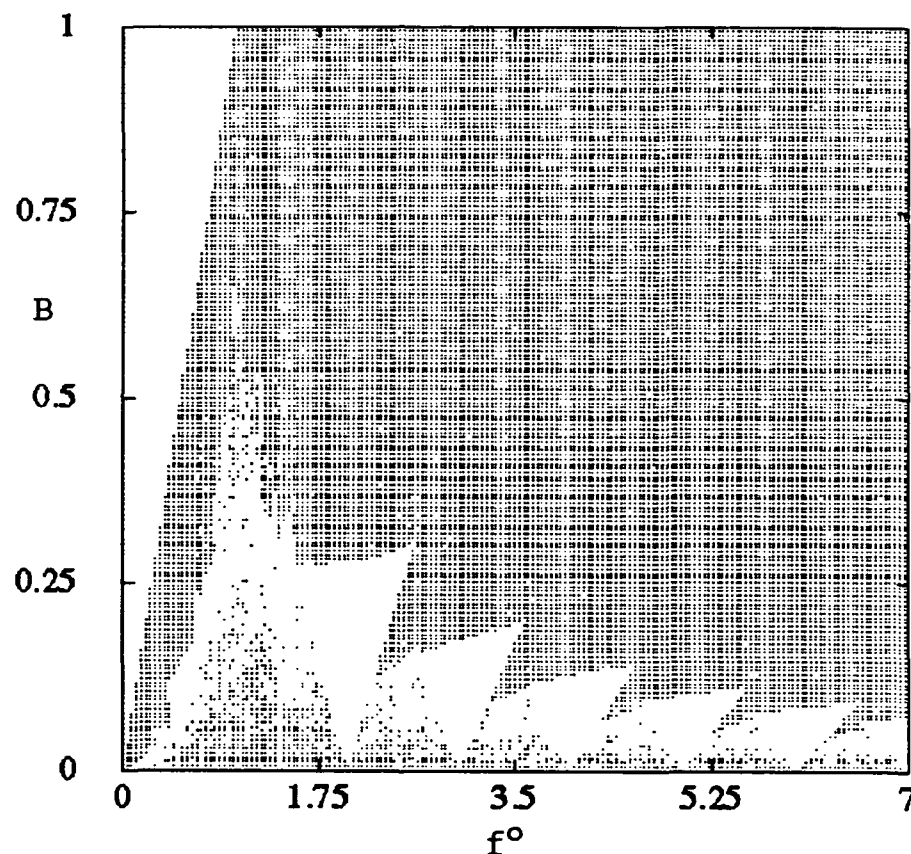


FIGURE 23.a Phase diagram for $B \equiv B_1 = B_2$ vs. f_0 .

It was shown in that work that there are extended systems where synchronized chaos corresponds to spatial order and temporal disorder. By varying the external parameters spatiotemporal chaos, or turbulence, may also appear.

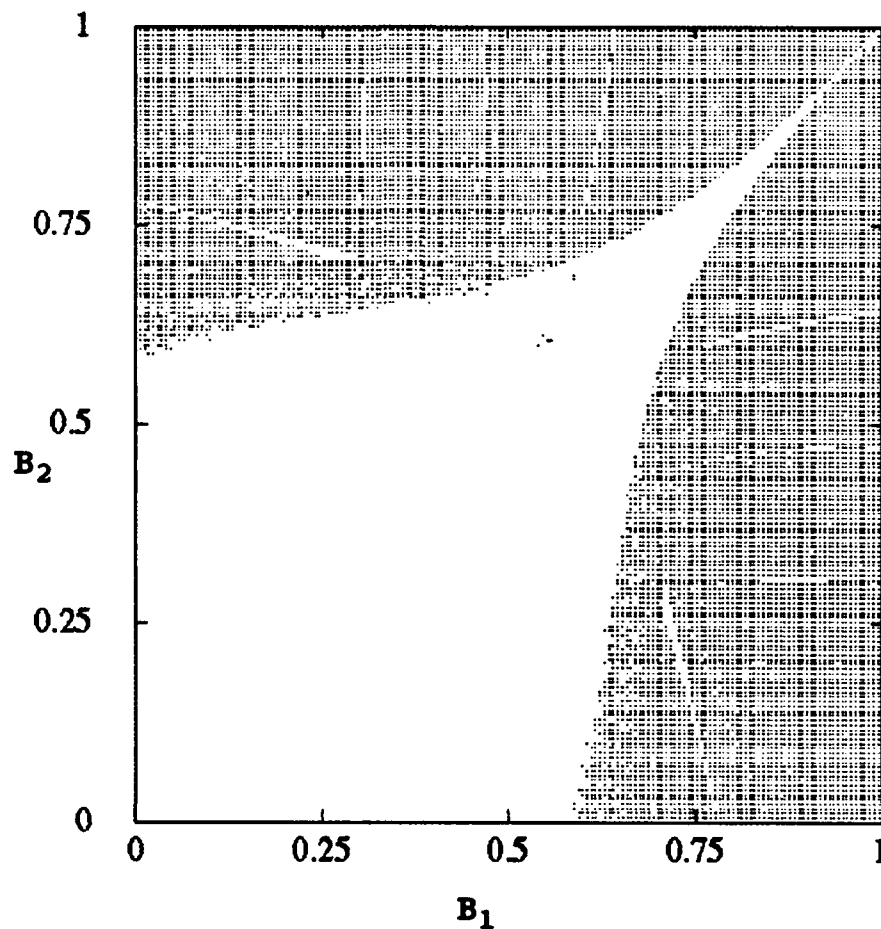


FIGURE 23. b Phase diagram for B_2 vs. B_1 for $f_0 = 1$ showing the nonperiodic region)

We first study the synchronization to a chaotic signal in a system of three coupled DPLLs. The transmitter consists of the two coupled loops studied in the previous sections and the receiver is third loop, which may be used to synchronize with one of the loops in the transmitter. The schematic of the system is shown in FIGURE 24. We observe numerically that if loops 1 and 3 are completely identical, then the synchronization between them is observed in determined regions of the parameter space, even when the transmitter is chaotic, as found in Refs. 1 and section 3.1. This occurs when the Liapunov exponents associated with loops 1 and 3 are

negative, and positive for loop 2.

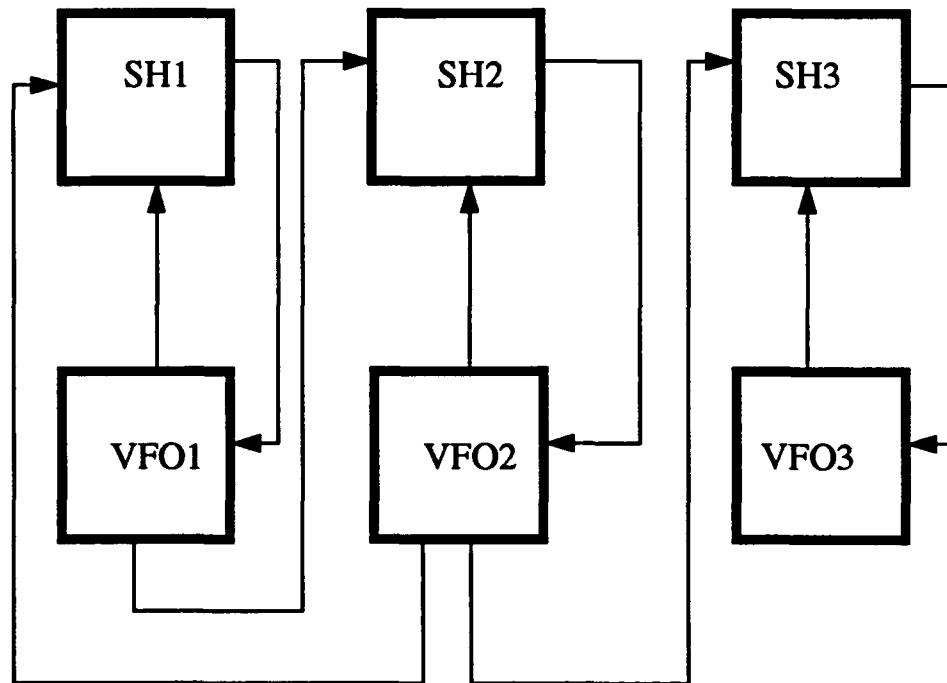


FIGURE 24. Communication system consisting of three coupled DPLLs

Due to the presence of more than one basin of attraction, or due to determined lack of symmetries in the system, loops 1 and 3 may not synchronize, as discussed below.

To demonstrate the synchronization between transmitter and receiver we plot in FIGURE 25. the outputs of loops 1 and 3 for the particular point $B_1=B_2=B_3=0.2$ and $f_1^0 = f_3^0 = 4$ where the transmitter has positive Liapunov exponent, and hence the phases ϕ_1 , ϕ_2 and ϕ_3 are chaotic. To check if the signal is indeed chaotic we use the algorithm given in Ref. 8. The quantities shown in the figure are ϕ_3 vs. ϕ_1 at $\phi_2=0$, and it is seen that the synchronization between loops 1 and 3 is perfect. Thus even with different initial conditions, as used in the simulations, the steady state temporal evolution of

loops 1 and 3 are completely identical.

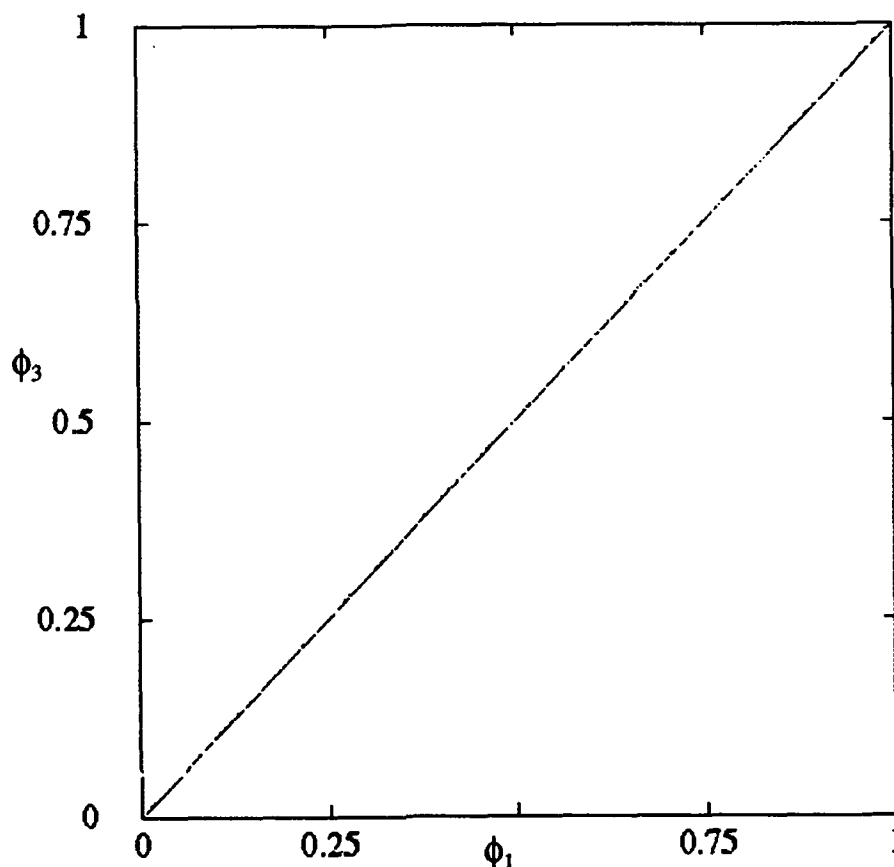


FIGURE 25. ϕ_3 vs. ϕ_1 at $\phi_2=0$ for $B_1 = B_2 = B_3 = 0.2$ and $f_1^o = f_3^o$

We show in FIGURE 26. a the regions (white) where synchronization is observed between loops 1 and 3 for $B_1=B_2=B_3 \equiv B$ in the plane B vs. f^o . The initial condition used was $\phi_1=0.1$, $\phi_2=0.3$ and $\phi_3=0.4$, and $f_1=f_2=f_3=1$. When Fig. 10(a) is compared with FIGURE 23.a, one sees that for regions where the transmitter has a periodic behavior, the synchronization between loops 1 and 3 is not observed. Note that the transmitter in our system consisting of a system of two coupled DPLLs is intrinsically different from the receiver, where the coupling is only in one direction. We observe that this lack of symmetry between the transmitter and receiver causes the nonsynchronization between loops 1 and 3 in the regions where periodic behavior exists in the transmitter, as well as in the receiver. For example, this is seen when B is small and f^o is close to an odd number in FIGURE 26. a. We checked with several sets of initial conditions and the synchronization of loops 1 and 3 was never obtained in these

periodic regions.

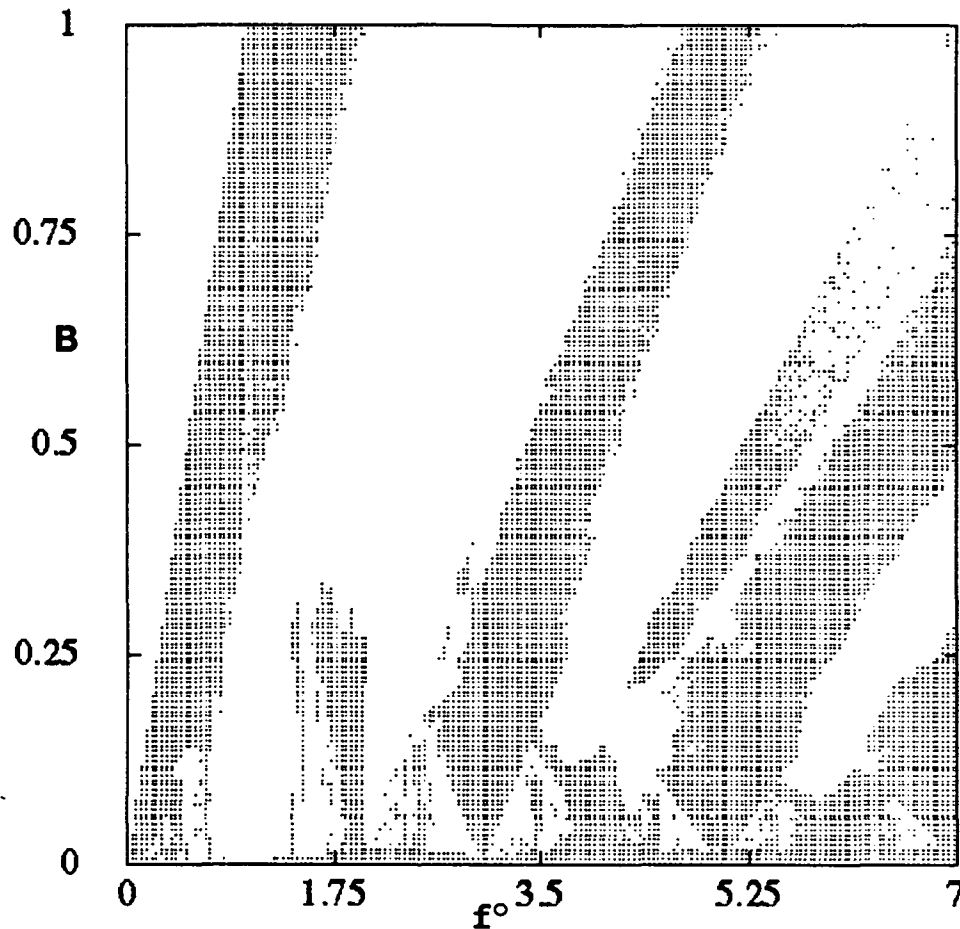


FIGURE 26. a Diagram showing the region of synchronization between loops 1 and 3 (white region) for $B \equiv B_1 = B_2 = B_3$ vs. f^0

In FIGURE 26.b we show the region (white) of synchronization between loops 1 and 3 for the plane B_2 vs. B_1 and $f^0=1$. We also observe nonsynchronization between loops 1 and 3 in the region where the transmitter is periodic. This occurs, for instance, for $B_2 > B_1$ and $B_2 \in [0, 0.5]$, where a cycle with period one is observed. The phase difference of loops 1 and 3 with respect to loop 2 is in this case given respectively by $\Delta\phi = 0.25$ and $\Delta\phi = 0.75$, and is found to be independent of the initial conditions. The nonsynchronization is again due to the lack

of symmetry between the first and the third loop.

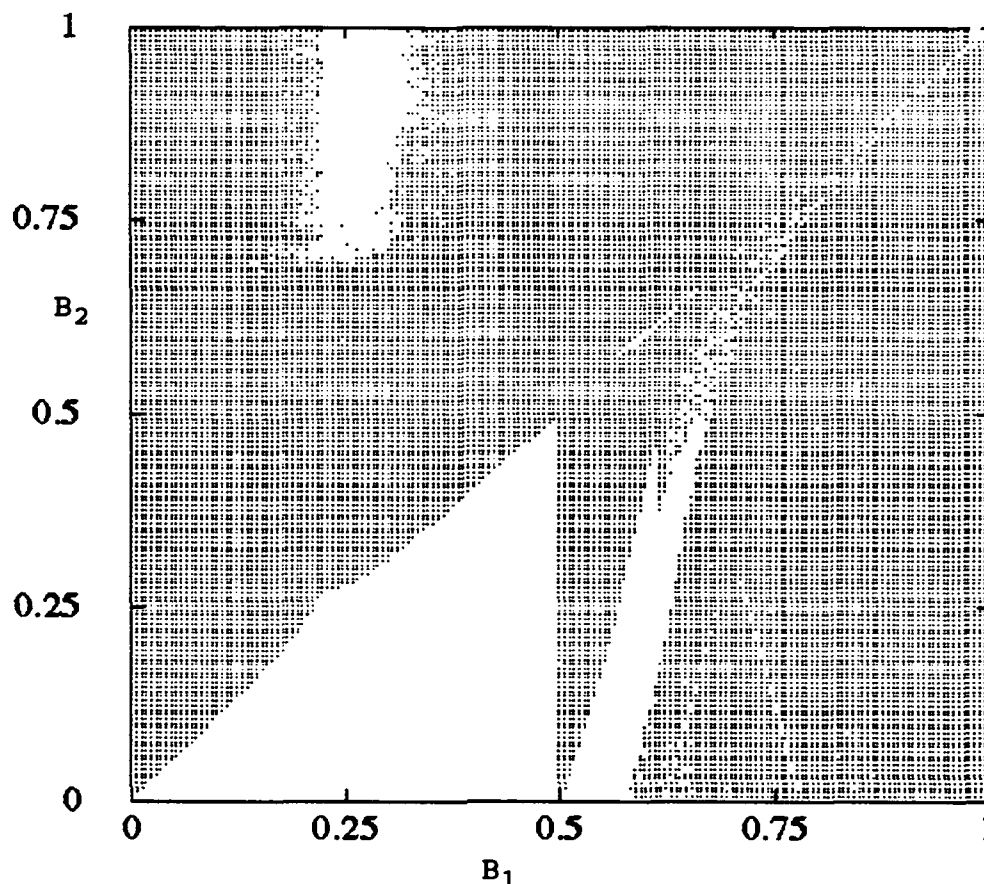


FIGURE 26.b Diagram showing the region of synchronization between loops 1 and 3 (white region) B_1 vs. B_2 for $\rho = 1$

The chaotic attractors obtained by plotting ϕ_3 vs. \bar{T}_3 , at $\phi_2=0$ are shown in FIGURE 27. a and FIGURE 27. b. The first case, FIGURE 27. a, corresponds to the strange attractor obtained for $B_1=B_2=B_3=0.2$ and $f_1^o = f_3^o = 4$, where loops 1 and 3 synchronize. In FIGURE 27. b the attractor for $B_1=B_2=B_3=0.4$ and $f_1^o = f_3^o = 3.5$ corresponds to nonsynchronization between receiver and transmitter. In the second case, the attractor seems to explore more regions of the phase space. It was noted in Ref. 9 that when synchronization between the master and slave systems occurs, then the dimensionality of the system as a whole is smaller than in the case the synchronization is not observed. This was shown by calculating

Liapunov dimensions.

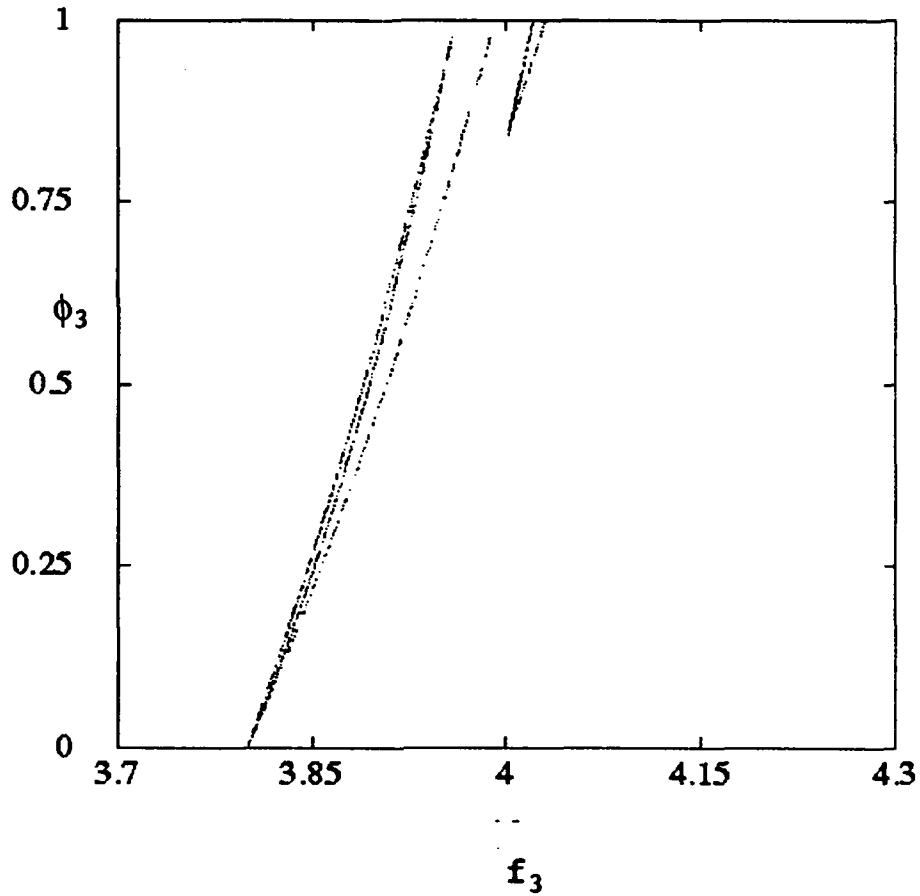


FIGURE 27. a Chaotic attractor ϕ_3 vs. f_3 at $\phi_2 = 0$ for $B_1 = B_2 = B_3 = 0.2$ and $f_1^0 = f_3^0 = 4$

We also confirmed this fact in our system by calculating the correlation dimension of the chaotic attractors for these two cases. The correlation dimension represents a lower bound to the number of independent variables necessary to describe or model the underlying dynamics of the attractor. In general, for chaotic attractors, if this positive defined dimension is a fractional number, then the bound is the next integer. Grassberger and Procaccia introduced an efficient algorithm to calculate the correlation dimension d_c , which is described in detail in Ref. 10. We calculated d_c for the attractors shown in FIGURE 27. a and FIGURE 27. b using the algorithm given in Ref. 10. We find for the synchronized case (FIGURE 27. a) $d_c \sim 1.1$. For the attractor shown in FIGURE 27. b we found $d_c \sim 2.5$. Thus the underlying dynamics for the communication system for these parameter sets can be described by two and three variables for the cases where synchronization and nonsynchronization is observed, respectively.

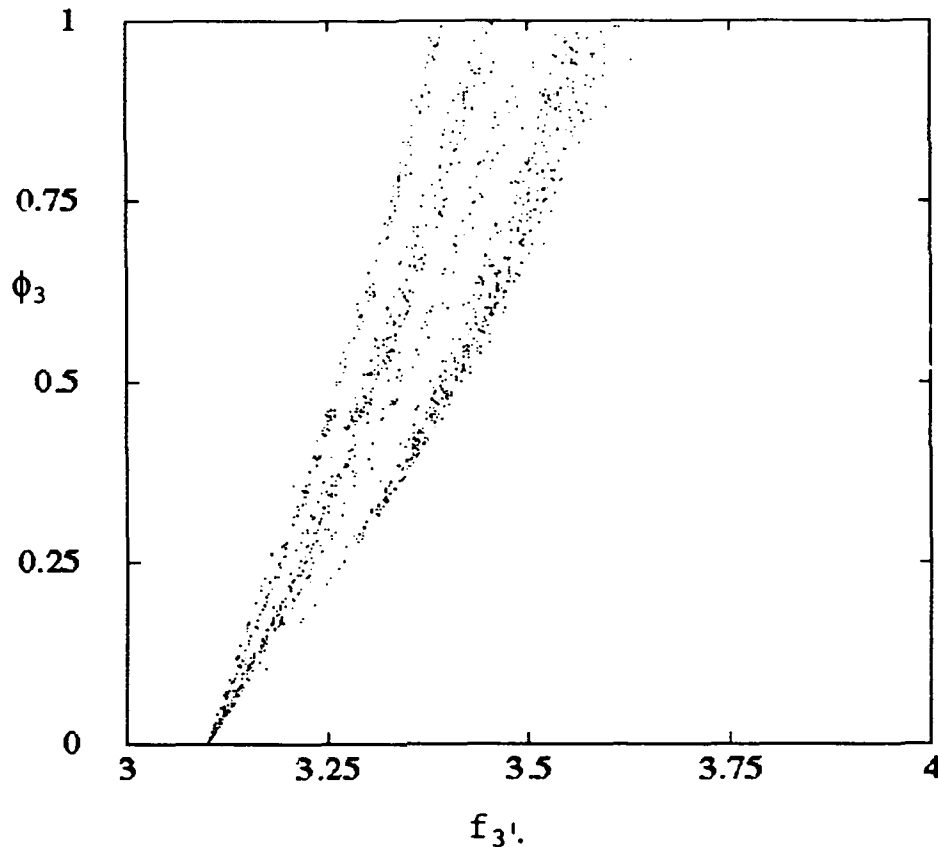


FIGURE 27. b Chaotic attractor ϕ_3 vs. f_3 at $\phi_2 = 0$ for $B_1 = B_2 = B_3 = 0.4$ and $f_1^0 = f_3^0 = 3.5$

3.2.5 QUANTIFICATION OF THE SYNCHRONIZATION

In a practical situation, it would not be possible to make the parameters of loops 1 and 3 completely identical. Pecora and Carroll observed that even in the case that the stable loops in the transmitter and receiver are not identical, the synchronization persists, but with some error between the dynamical values of the master and slave system. This may be an undesirable property for secure communication applications.

In our simulations we observed that the degree of correlation between the transmitter and receiver strongly depends on the parameter that is being varied. For our system making the center frequency f_3^0 slightly different, say 1%, from f_1^0 , loops 1 and 3 become practically uncorrelated, as seen in. Whereas, if we vary the gain B_3 by a much larger relative amount with respect to B_1 , the degree of correlation between loops 1 and 3 remains high, as shown in FIGURE 28. b.

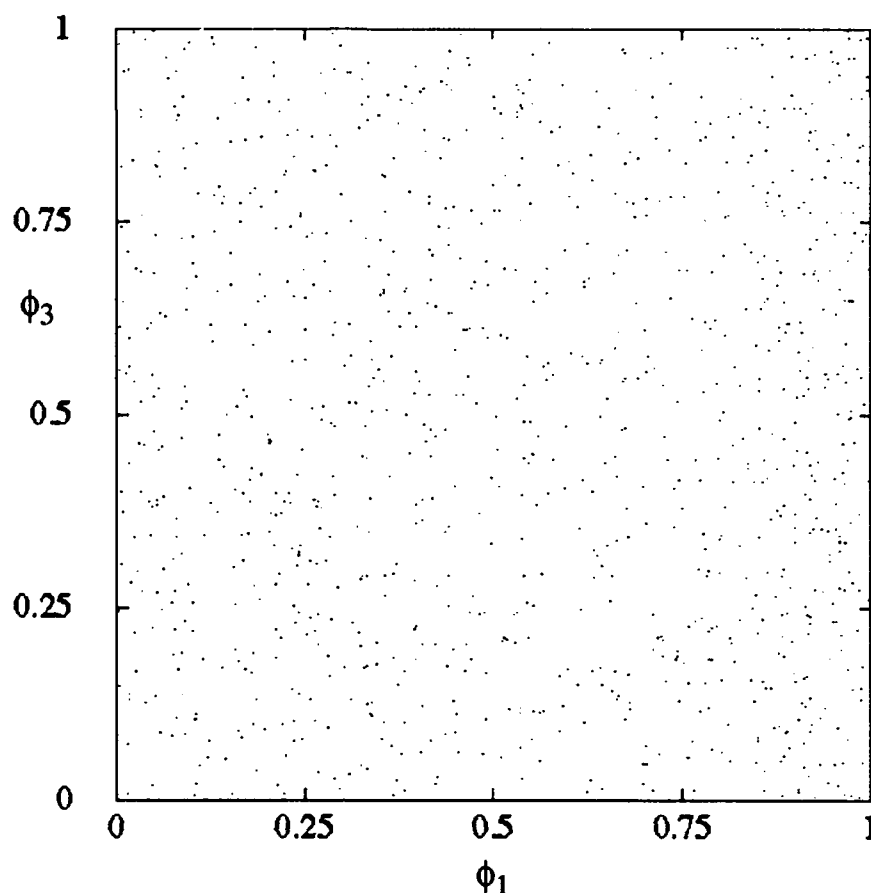


FIGURE 28. a ϕ_3 vs. ϕ_1 at $\phi_2 = 0$ for $B_1 = B_2 = B_3 = 0.2$ and $f_1^0 = 4, f_3^0 = 4.04$

We use the concept of mutual information to quantitatively characterize the degree of correlation between the transmitter and receiver when linked by the same chaotic signal. The concept of mutual information was introduced by Shannon¹¹ as a quantitative measure of the general dependence between two variables. If two variables are independent, the mutual information between them is zero. If the two variables are strongly dependent, the mutual information between them is large. It is well known that the mutual information is a better quantity to measure dependence than the correlation function, which only measures the linear dependence. We begin by briefly reviewing the basic definition of mutual information^{11,12}. Consider a dynamical system that is described by the discrete variable X_1 and that this system has relaxed to an attractor. One starts by dividing the phase space of X_1 into N boxes. Denote by $p(i_1)$ the probability that a measurement of the system will find the variable X_1 in the

ith box. Do the same for X_2 . If two systems are measured simultaneously, then the relevant probability distributions are $p(i_1)$, $p(i_2)$, and the joint probability distribution $p(i_1, i_2)$

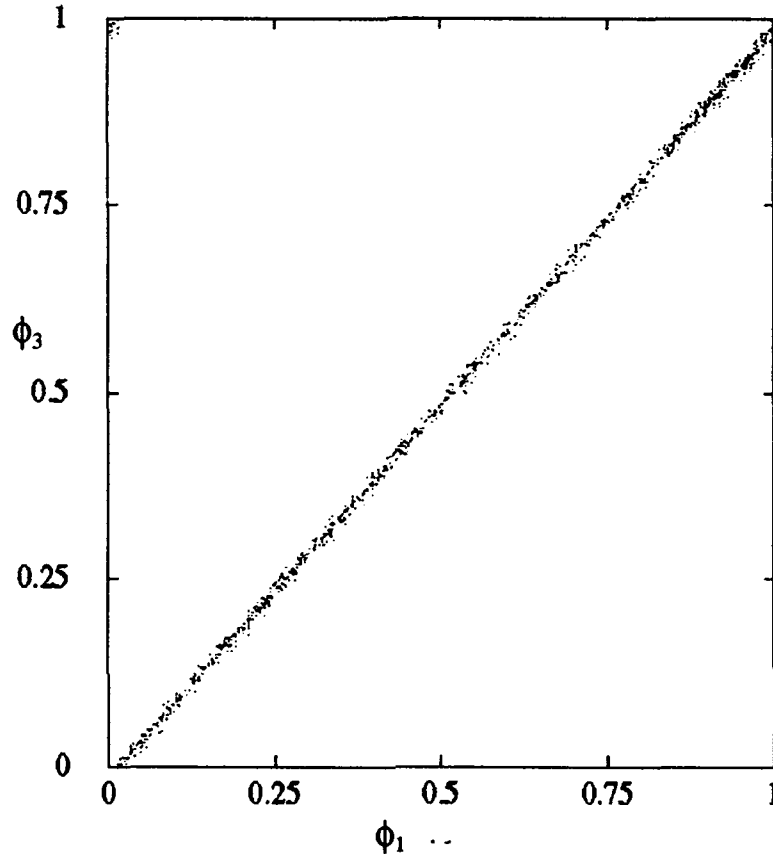


FIGURE 28. b ϕ_3 vs. ϕ_1 at $\phi_2 = 0$ for $B_1 = B_2 = 0.2$, $B_3 = 0.25$ and $f_1^0 = 4, f_3^0 = 4$.

The mutual information is defined as

$$I(X_1, X_2) = \sum_{i_1, i_2} p(i_1, i_2) \ln_2 \left[\frac{p(i_1, i_2)}{p(i_1)p(i_2)} \right] \quad (33)$$

where the sum extends over all elements of the joint partition for which $p(i_1)$ and $p(i_2)$ are both nonzero. The mutual information gives the amount of information gained, in bits, about one system from a measurement of the other. It is a dynamical invariant, i.e., it does not depend on the system of coordinates used. When the number of cells of the phase space partition N is increased, the resolution of measurement

is also increased, as well as the information about the state of the system. Consequently, the mutual information will depend on N . If X_1 and X_2 are independent, then $p(i_1, i_2) = p(i_1)p(i_2)$ and $I(X_1, X_2) = 0$.

Mutual information was recently used in Ref. 10 in the context of chaotic synchronization. It was shown that the mutual information is large when two subsystems are operating in the regime of chaotic synchronization, as described above, which corresponds to the regime of spatial order and temporal disorder. The mutual information rapidly decreases to a small value when all subsystems are operating in the chaotic regime, which corresponds to spatiotemporal chaos.

We calculated the mutual information for the three loop system shown in FIGURE 24. We also calculated a normalized mutual information using the following definition

$$I'(X_1, X_2) = \frac{I(X_1, X_2)}{\sum_{i_1, i_2} p(i_1, i_2) \ln_2 p(i_1, i_2)} \quad (34)$$

Thus, if the outputs of systems 1 and 2 are completely identical, then $p(i_1, i_2) = p(i_1) = p(i_2)$, and $I'(X_1, X_2) = 1$. We analyzed two cases described below. In all of them we used 30,000 points in the computation after the transient died. We divided the interval $[-1, 1]$ (range of the voltage signal) into 200 boxes. The data used in the calculation are the values of the voltage of the signals of loops 1 and 3 when loop 2 samples. If we use the phase as the variable studied, instead of the voltage, the results obtained are very similar to the ones that we will show.

In the first case we take $B_1 = B_2 = B_3 = 0.2$, $f_1^0 = 4$ and vary f_3^0 . We show in FIGURE 29. a I vs. f_3^0 . The mutual information between loops 1 and 3 is large only when the difference between their center frequencies is very small or null. The mutual information attains its maximum at $f_1^0 = f_3^0$ where the transmitter and receiver are completely synchronized. At this point $I' = 1$. We observe that I and I' are small and approximately constant if the center frequencies of loops 1 and 3 are not identical (or almost identical) except for $f_3^0 \approx f_2^0 = 1$. This indicates that parameter matching between loops 2 and 3 increases the correlation between transmitter and receiver. This is in some sense expected, since loop 1 is fed by loop 2.

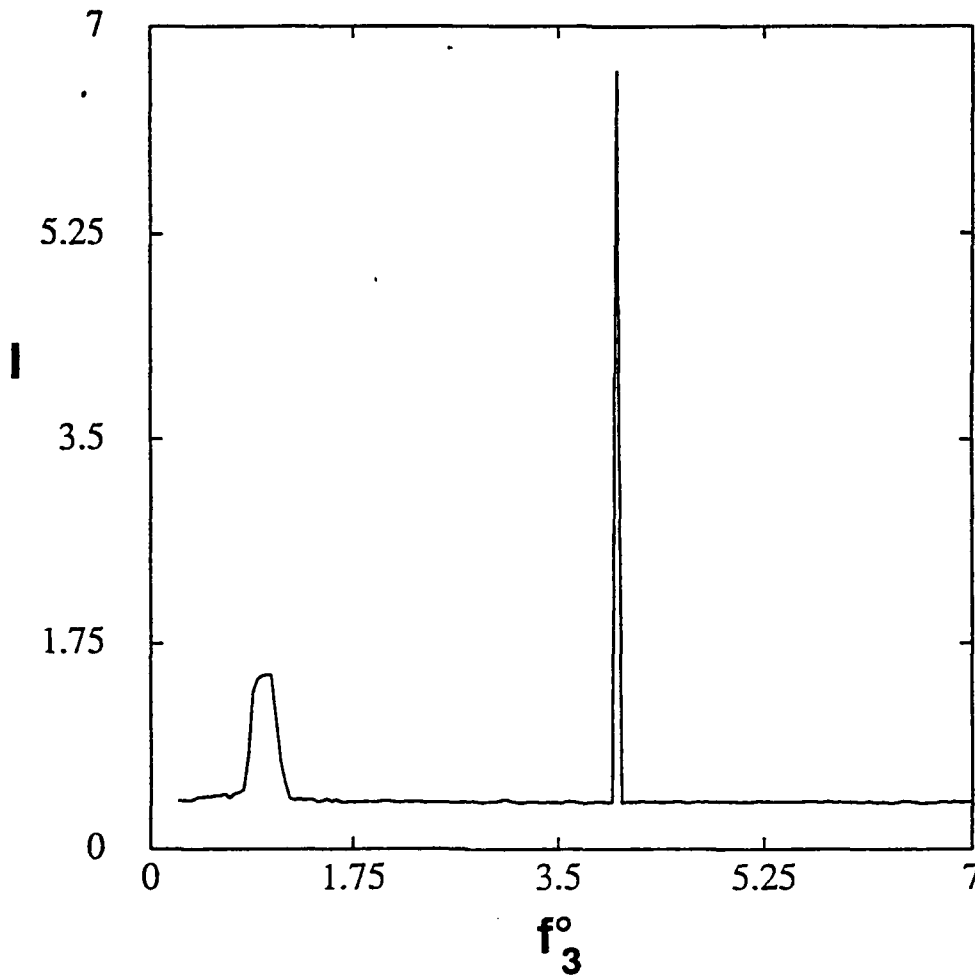


FIGURE 29. a Mutual information between loop 1 and loop 3; I vs. f_3^o for $B_1 = B_2 = B_3 = 0.2$ and $f_1^o = 4$

Now let us examine the mutual information for another plane of the parameter space. We take $f_1^o = f_3^o = 4$, and $B_1 = B_2 = 0.2$ and vary B_3 . The mutual information between loops 1 and 3 for this example is shown in FIGURE 29. b. Again the maximum of I and I' occurs when loops 1 and 3 are identical, and in this case $I' = 1$. On the other hand, unlike the case studied in the last paragraph, the mutual information between loops 1 and 3 decreases quite slowly when the difference $|B_1 - B_3|$ increases.

This implies that if for security reasons one needs a communication system that is very sensitive to variations in the parameters, then the center frequency value could be used as a key. On the other hand, if one operates in a very noisy environment, then the gain might be better for this purpose. In this case, one can make the system complicated enough, e.g. by adding other loops in the transmitter and receiver, in

order to make more difficult the interception of the message. This is discussed in the next section.

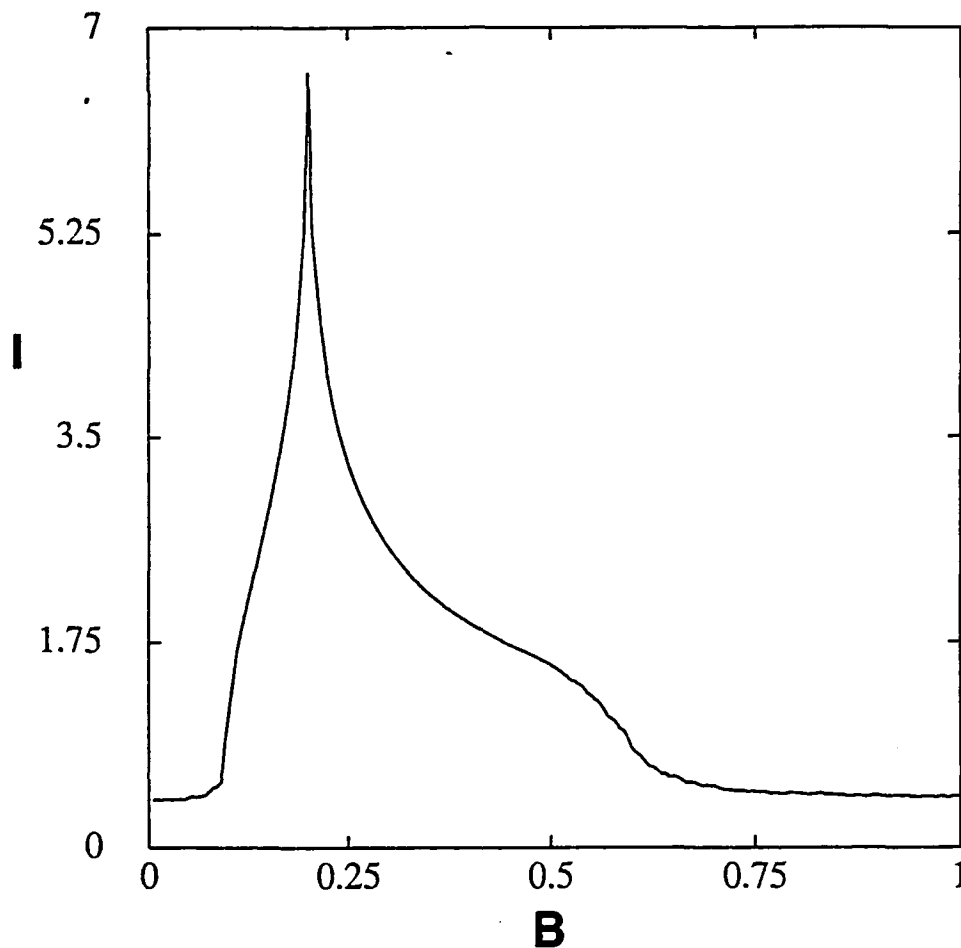


FIGURE 29. b Mutual information between loop 1 and loop 3; I vs. B_3 for $B_1 = B_2 = 0.2$ and $f_1^0 = f_3^0 = 4$

3.2.6 MORE COMPLEX SYSTEMS

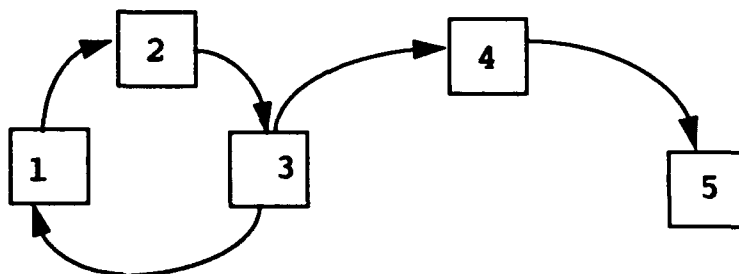


FIGURE 30. Communication system consisting of 5 loops

We tested the idea of chaotic synchronization in a more complex system (shown in FIGURE 30.), where the transmitter consists of three loops and the receiver of 2 loops. Thus, for the receiver we have four control parameters governing its behavior, i.e., two center frequencies and two gains. By normalizing the parameters we may take, without loss of generality, $f_3^o = 1$. Consequently the complete system, transmitter plus receiver, has a total of 9 parameters. We verified that only in the case that loop 1 and loop 2 are completely identical to loops 4 and 5, respectively, that perfect synchronization between loops 2 and 5 is achieved as well as between loops 1 and 4.

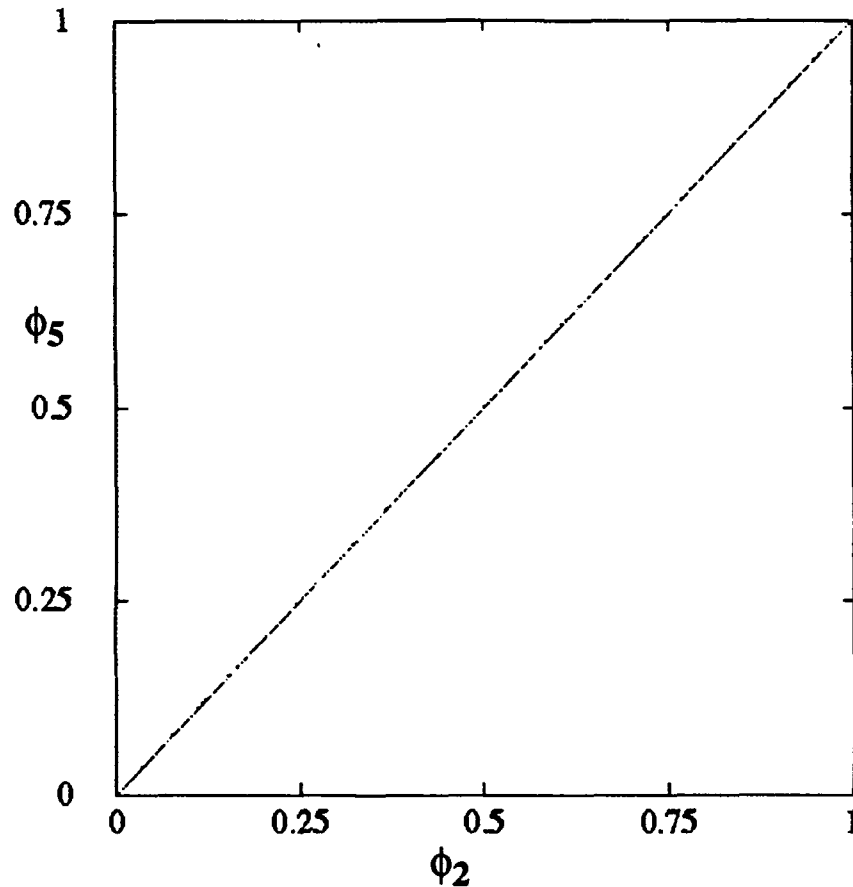
In FIGURE 26.a, we show the phase output of loops 2 and 5 for a typical example, that is, $B_1 = B_2 = B_3 = B_4 = B_5 = 0.2$, $f_1^o = f_4^o = 4$ and $f_2^o = f_5^o = 5$. The synchronization between transmitter and receiver is perfect in this case. If one of the loops 4 or 5 is not identical to its respective loop in the transmitter, then the synchronization is seriously affected, as shown in FIGURE 26. b, where the parameters are identical to those ones taken in FIGURE 26.a, except for $f_4^o = 4.05$.

More complex configurations could be imagined. However we argue that no chaotic loop should exist in the receiver. If there is a chaotic loop in the receiver, then due to the sensitivity to the initial conditions we do not expect synchronization between the receiver and the transmitter, even if there is parameter matching. In this case, an infinitely small difference in the initial conditions between the transmitter and the receiver will increase exponentially in time. On the other hand, the existence of several chaotic loops in the transmitter may be a desirable configuration, for security reasons, since this could make the transmitted signal look more chaotic, having a higher dimension, as seen in FIGURE 27. a and FIGURE 27. b.

3.2.7 CONCLUSIONS

We studied the synchronization to a chaotic signal in a system of coupled DPLL's. Our transmitter consists of two self-synchronized DPLL's, loops 1 and 2, and the receiver consists of a third loop. The phase diagram of the transmitter and the region of synchronization between loops 1 and 3 was studied numerically for some planes of the parameter space. We used the concept of mutual information to quantify the degree of correlation between transmitter and receiver. We verified that if the center frequencies of loops 1 and 3 are not completely identical (or almost identical) the synchron-

ization between them strongly degraded. Whereas, a quite large difference between the gains of the loops only weakly affects the synchronization.



Finally, we investigated a more complex system consisting of five coupled DPLL's. We showed that only when the stable part of the transmitter is completely identical to the receiver, the is perfect synchronization between them is observed

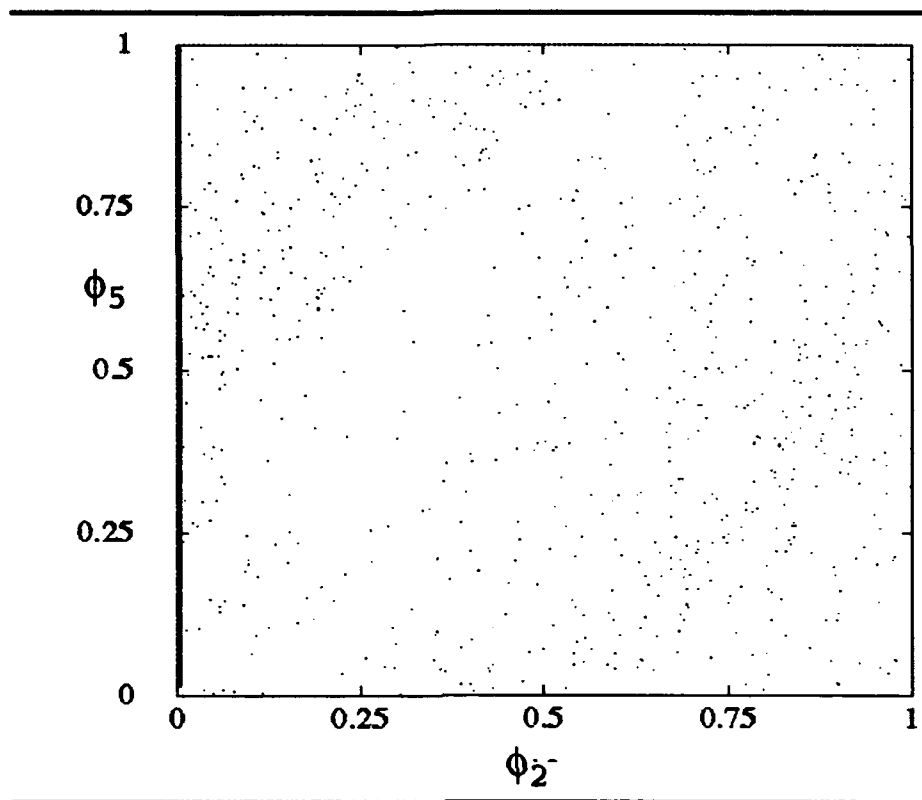


FIGURE 30. b ϕ_5 vs. ϕ_2 at $\phi_3 = 0$ for $B_1 = B_2 = B_3 = B_4 = B_5 = 0.2$
 $f_1^0 = 4$, $f_4^0 = 4.05$, $f_2^0 = f_5^0 = 5$

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3.3 Mapping Equations

We derive mapping equations for the coupled digital phase-locked loop (DPLL) system. The phase space we will derive will be 3-dimensional, with each state having a convenient interpretation. The mapping equations will be differentiable everywhere except on a two-dimensional planar subspace. We show that these equations, and hence the dynamics of the coupled digital PLL's are generalizations of the dynamics of a bouncing ball on a large periodically-varying table, a system which has been studied by several authors. We show that no fixed points exist in this map, but that period-two points do exist.

To begin, we define mapping equations for the system. We describe the dynamics of the loops at the sampling time of either loop. Consider the n th sample, and define the following times

$$\begin{aligned} a_n &= \text{time until loop 0 next samples} \\ b_n &= \text{time since loop 0 last sampled} \\ c_n &= \text{time until loop 1 next samples} \\ d_n &= \text{time since loop 1 last sampled} \end{aligned} \tag{35}$$

If loop 0 is sampling at n , define $b_n = 0$, while if loop 1 is sampling at n define $d_n = 0$. It is clear that the evolution of these four time variables uniquely describes the dynamics of the coupled PLLs. Note, however, that for all n , we must have either $b_n = 0$, or $d_n = 0$. So although the phase space appears to be \mathcal{R}^4 , the dynamics really live on the intersection of the two three-dimensional linear subspaces ($b_n = 0$ and $d_n = 0$) of \mathcal{R}^4 . If we remove $b_n = d_n = 0$ from consideration, then the dynamics live on a (disconnected) three dimensional subset of \mathcal{R}^4 . We will show how to parametrize this subspace globally by defining a new set of variables based on linear combinations of a_n , b_n , c_n and d_n .

First, we write down the evolution equations in terms of the variables in eq (35). T_0 and T_1 are the period functions of loops 0 and 1 respectively, where $T_i: S^1 \rightarrow \mathcal{R}^+$ and $S^1 = \mathcal{R} \pmod{1} = \{[x] : 0 \leq x < 1, x \equiv y \text{ if } x - y \in \mathcal{Z}\}$. In a real DPLL system, $T_0(\phi) = T(b_0, \phi)$ and $T_1 = T(b_1, \phi)$ where $T: \mathcal{R} \times S^1 \rightarrow \mathcal{R}^+$, is another period function that depends on some (static) external parameter b . The idea will eventually be to vary b_0 and b_1 for relevant T functions and investigate the subsequent dynamics. For now, we may assume that T_0 and T_1 are arbitrary period functions.

Writing the mapping equations is complicated by the fact that they change depending on whether loop 0 or loop 1 samples at $n+1$. This situation causes the phase-space discontinuity mentioned earlier. Fortunately, the variables in eq (35) provide a simple means for determining which loop will sample at $n+1$. In particular, if $a_n - c_n < 0$ loop 0 will sample next, while if $a_n - c_n > 0$ loop 1 will sample next. In the first case (loop 0 next samples), the next-state equations are

$$\begin{aligned}
a_{n+1} &= T_0 \left(\frac{a_n + d_n}{c_n + d_n} \right) \\
b_{n+1} &= 0 \\
c_{n+1} &= c_n - a_n \\
d_{n+1} &= a_n + d_n
\end{aligned} \tag{36}$$

In the other case (loop 1 next samples) they are

$$\begin{aligned}
a_{n+1} &= a_n - c_n \\
b_{n+1} &= c_n + b_n \\
c_{n+1} &= T_1 \left(\frac{a_n + d_n}{c_n + d_n} \right) \\
d_{n+1} &= 0
\end{aligned} \tag{37}$$

Note that at all samples n , we have $b_{n+1} = 0$ or $d_{n+1} = 0$. Hence, as mentioned above, all iterates lie in a three dimensional subspace of our four-dimensional space. We can parameterize this space observing that in order to evolve the above equations we need to know only the following linear combinations of parameters:

$$\mathbf{P} = \{a_n + d_n, c_n + d_n, c_n - a_n, a_n + b_n, c_n + b_n\}.$$

Regarding $\{a_n, b_n, c_n, d_n\}$ as basis vectors in \mathcal{R}^4 , we see that the span of \mathbf{P} is three-dimensional. In particular,

$$\text{span} \{a_n - c_n, a_n + b_n, c_n + d_n\} = \text{span}\{\mathbf{P}\}$$

Hence, if we define

$$\begin{aligned}
X_n &= a_n - c_n \\
Y_n &= a_n + b_n \\
Z_n &= c_n + d_n
\end{aligned} \tag{38}$$

we may write the mapping equations in (36) and (37) respectively as

$$\begin{aligned}
X_{n+1} &= X_n + T_0 \left(1 + \frac{X_n}{Z_n} \right) = X_n + T_0 \frac{X_n}{Z_n} \\
Y_{n+1} &= T_0 \left(1 + \frac{X_n}{Z_n} \right) = T_0 \frac{X_n}{Z_n} \\
Z_{n+1} &= Z_n
\end{aligned} \tag{39}$$

and

$$\begin{aligned}
X_{n+1} &= X_n + (-T_1) \left(1 - \frac{X_n}{Y_n} \right) = X_n + T_1 \frac{X_n}{Y_n} \\
Y_{n+1} &= Y_n \\
Z_{n+1} &= T_1 \left(1 - \frac{X_n}{Y_n} \right) = T_1 \left(-\frac{X_n}{Y_n} \right)
\end{aligned} \tag{40}$$

where eq (39) is used when $X_n < 0$ and eq (40) is used when $X_n > 0$. The second equations for X and Y in eq (39) and X and Z in eq (40) follow because T_i is defined on the circle S^1 . Finally, we use the step function $U : \mathcal{R} \rightarrow [0, 1]$, $U(t) = 1$ for $t > 0$, $U(t) = 0$ for $t < 0$ to "glue" the above two equations together, yielding

$$\begin{aligned}
X_{n+1} &= U(X_n) \left[X_n - T_1 \left(1 - \frac{X_n}{Y_n} \right) \right] + U(-X_n) \left[X_n + T_0 \left(1 + \frac{X_n}{Z_n} \right) \right] \\
Y_{n+1} &= U(X_n) Y_n + U(-X_n) \left(T_0 \left(1 + \frac{X_n}{Z_n} \right) \right) \\
Z_{n+1} &= U(X_n) \left(T_1 \left(1 - \frac{X_n}{Y_n} \right) \right) + U(-X_n) Z_n
\end{aligned} \tag{41}$$

Equation eq (41) completely describes the dynamics of the coupled DPLL system. Of course the state variables used in eq(38) are not unique; we could have used any three that spanned \mathcal{P} . However, the ones we have used have simple physical interpretations. For ex-

ample, the sign of X_n determines which loop (0 or 1) samples at the $n+1$ st sample. In particular, we may define the **sampling itinerary** of a trajectory starting from an initial condition $S_0 = \{X_0, Y_0, Z_0\}$ as the sequence $I(S_0) = \{U(X_n), n=0, \dots, \infty\}$, where $U(\bullet)$ is the step function defined above. The itinerary defined in this way records the sampling order of a trajectory starting from the initial condition S_0 . The Y_n variable can be interpreted as the **period** of loop 0 during the n th sample. If loop 0 is sampling at n , then Y_n is just the time until loop 0 will next sample. Similarly, Z_n can be interpreted as the period of loop 1 during the n th sample of the system.

Several other aspects of eq(41) are important. First, all three states are time variables, so that the phase space is \mathcal{R}^3 . More precisely, allowable iterates lie in the three-dimensional space $X < Y, -X < Z$. Furthermore, there is a discontinuity in the map on the plane $X=0$, which corresponds to the condition of both loop 0 and loop 1 trying to sample. Keeping the dynamics away from $X = 0$ is an important requirement we shall consider later. For now, we shall ignore this consideration. Also note that eq(41) is invariant under the transformation

$$\begin{aligned} X_n &\rightarrow -X_n \\ Y_n &\rightarrow -Z_n \\ Z_n &\rightarrow -Y_n \\ T_n &\rightarrow -T_{1-i} \quad i = 0, 1 \end{aligned} \tag{42}$$

a fact which may be verified directly, but which is obvious from the physical interpretation of X, Y , and Z . This transformation amounts to **renaming** loop 0 and loop 1. Finally, note there are no fixed points of eq (41). This may also be verified directly, but, observe that if fixed points existed, then one loop (either loop 0 or loop 1) would sample at each n (i.e., $I(S_0)(n) \equiv U(X_0)$). But this is impossible, since we require each loop to be operating at nonzero frequency, and we insure this by requiring $T_i > 0, i = 1, 2$ on their domains of definition.

Period-two points do exist, however. Such points have trajectories with sampling itineraries $\{10\dots\}$, or by the renaming transformation in eq (42), $\{01\dots\}$. So without loss of generality, we seek period-two points whose trajectories have $\{10\dots\}$ sampling itinerary. Knowledge of the itinerary allows us to easily compute the 2nd iterate of eq (41) and we find that period-two points are those X, Y , and Z which satisfy the implicit nonlinear equations

$$X = T_1 \left(1 - \frac{X}{Y}\right) \quad (43)$$

$$Y = T_0 \left(\frac{X}{Z}\right)$$

$$Z = Z$$

Whether solutions of these equations exist of course depends on T_0 and T_1 . We shall analyze eq (43) for two cases that are found in "real" digital phase-locked loops; first, where the VCO oscillates with sine-wave output;

$$T(b_i, \phi) = T_i(\phi) = \frac{1}{1 + b_i \sin(2\pi\phi)}$$

and second where the VCO oscillates with a triangular-wave output

$$T(b_i, \phi) = T_i(\phi) = \frac{1}{1 + b_i \Lambda(2\pi\phi)}$$

where $\Lambda: S^1 \rightarrow [-1,1]$ is the standard piecewise-linear triangle function.

$$\Lambda(\phi) = \begin{array}{ll} 4\phi & 0 \leq \phi \leq 1/4 \\ 2 - 4\phi & 1/4 \leq \phi \leq 3/4 \\ 4\phi - 4 & 3/4 \leq \phi \leq 1 \end{array}$$

In both cases above the b_i are static external parameters.

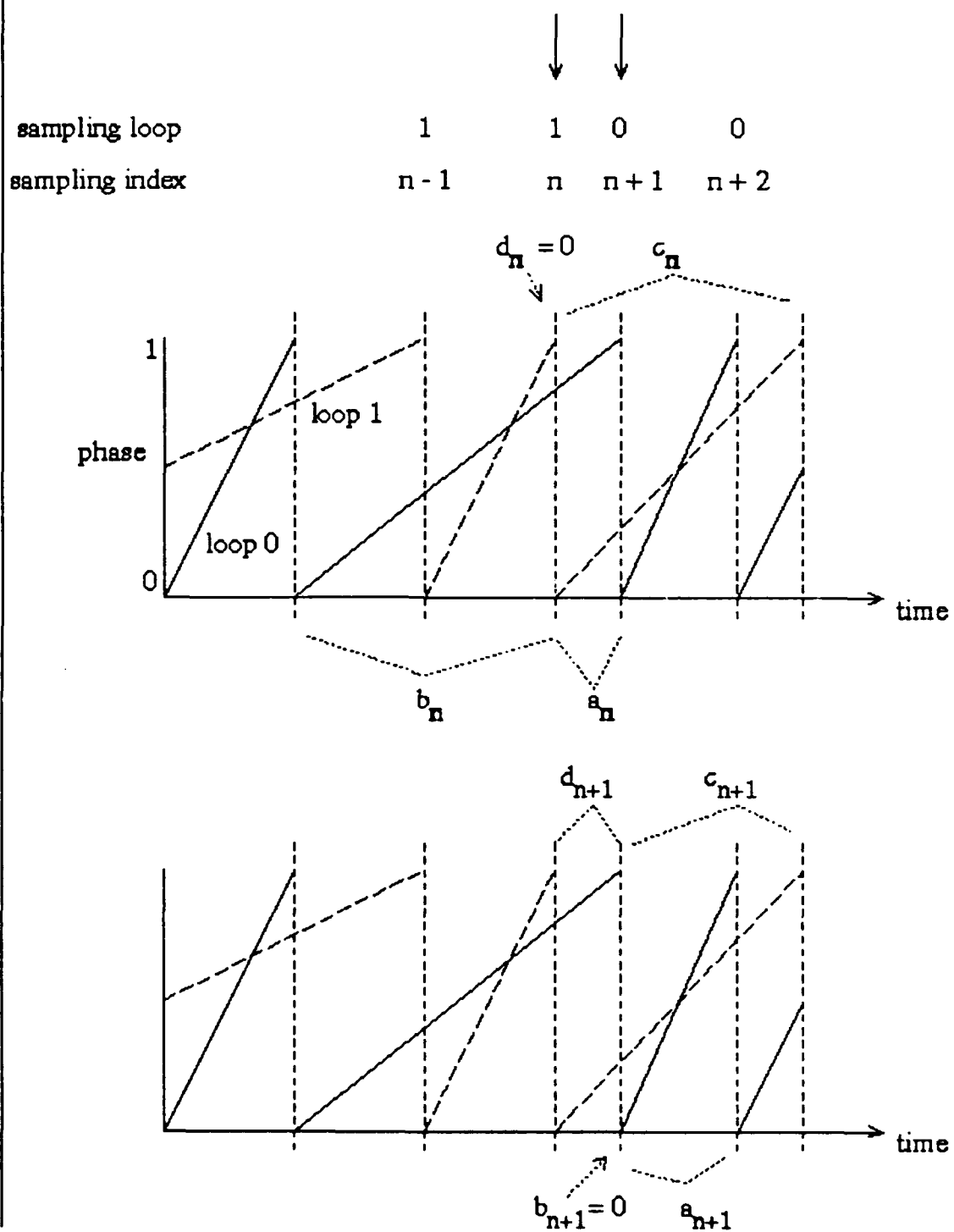


FIGURE 31. State variables for coupled DPLLs

3.4 Digital Data Transmission System Using Two Coupled DPLL

3.4.1 Introduction

It has been shown elsewhere in this report (see sections 3.1 and 3.2) that for the system of FIGURE 32. (shown below) the output of the VCOs of the first and third DPLLs can be synchronized in phase for all time, provided that the second loop has positive Lyapunov exponent and the other two loops have the identical coupling coefficients with negative Lyapunov exponents. A communication system having a similar configuration can be used for the transmission of binary data sequences. FIGURE 33. shows one such communication system. The coupled first and second DPLLs constitutes the transmitter and the third and fourth DPLLs make up the receiver.

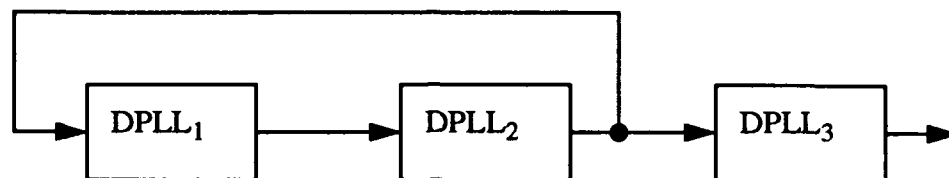


FIGURE 32. A Chaotic Dynamical System Using Coupled Digital Phase Locked Loop With Second Loop Having Positive Lyapunov Exponent

In the system of FIGURE 33. the second DPLL has its coupling coefficient set very high so that the loop has a positive Lyapunov exponent. The value of the coupling coefficient for the first loop is small so that the loop has a negative Lyapunov exponent. In addition, the coupling coefficient of the first loop is made to take on two different values; one value for the binary digit of a 1-bit, and another value for a 0-bit. Only the output of the VCO of the second DPLL is transmitted to the receiver and provided (in identical form) as inputs to the third and fourth DPLLs. The difference between the third and fourth DPLLs lies in their coupling coefficients. Namely, the coupling coefficient for the third DPLL matches that for 1-bit used for the first DPLL and that for the fourth DPLL matches that for 0-bit. Hence, when a 1-bit is transmitted, the output of the first DPLL will be in phase synchronization with that of the third DPLL. On the other hand, when a 0-bit is transmitted, the outputs of the first and the fourth DPLLs will be in synchronization,

3.4.2 Search For A Sub-optimal Decision Variable.

A decision variable, which is to be used in determining whether the transmitted bit is a zero or one, must be devised for this system. This variable, in the absence of thermal noise at the input, must unambiguously extract the 1 bit or 0 bit embedded in the signal. Since the output of first DPLL is not available at the receiver, the decision variable can only be based on the received signal (which is the output of the second DPLL) or certain variables related to the third and fourth DPLLs.

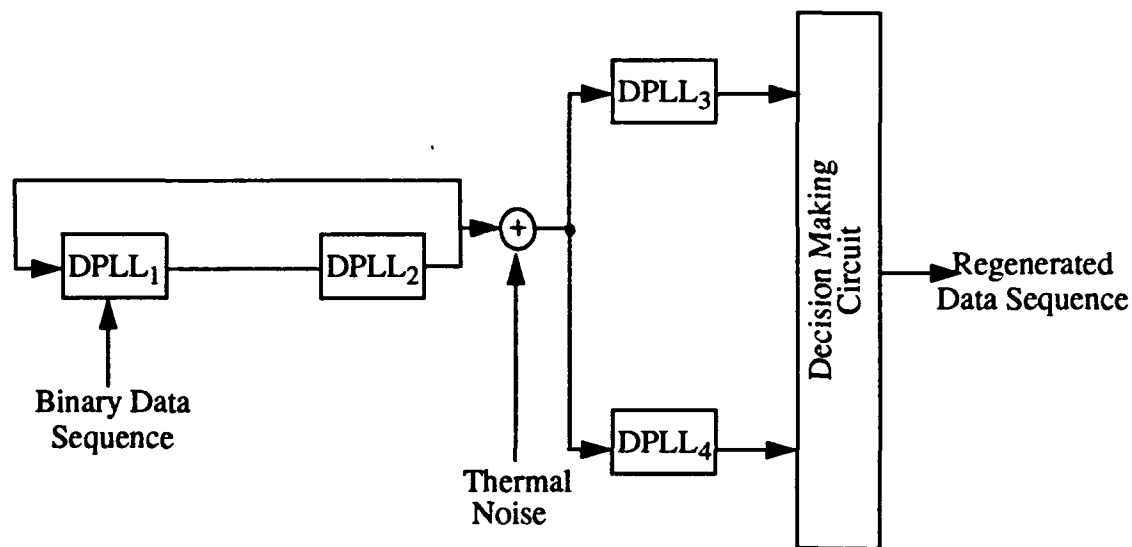


FIGURE 33. A Digital Communication System Employing Coupled Digital Phase Lock Loop With The Second Loop Having Positive Lyapunov Exponent

The decision variable is defined to be

$$D = V_{\text{matched}} - V_{\text{mis-matched}}$$

Where V_{matched} is the measured value of a property of whichever DPLL (the third or fourth) matched the coupling coefficient of the first DPLL, and $V_{\text{mis-matched}}$ is the measured value of the same property of the remaining DPLL (whose coupling coefficient did not match that of the first DPLL). The properties that have been investigated in this study are:

1. Input voltages at the third and fourth DPLLs at their respective sampling time instants.
2. The phase angles of the incoming signal at the third and fourth DPLLs sampling time instants.
3. Error voltages to the VCOs of the third and fourth DPLLs at their respective sampling time instants.
4. Frequencies of the third and fourth DPLLs at their respective sampling time instants.
5. Voltages or phase angles of the third and fourth DPLLs at the positive zero-crossings of the second DPLL output.
6. The first or second differences of one of the measured values of the properties listed above. Where the first and second differences of a successive measured values of the property, $\{v(-j), v(-j+1), \dots, v(-1), v(0), v(1), v(2), \dots\}$, are defined below.

First Difference of $v(i)$:

$$\Delta v(i) = v(i) - v(i-1)$$

Second Difference of $v(i)$

$$\Delta^2 v(i) = v(i) - 2 \times v(i-1) + v(i-2)$$

Where $\{v(i)\}$ is the sampled measurement of the property $\{v(1), v(2), v(3), \dots\}$.

The result of investigation indicates that property 2 above is the most suitable one to use. The decision variable formed from the difference between the cumulative sum of the successive absolute values of the second differences of property 2 remains positive for all the simulation runs independent of the initial conditions of the DPLLs. No such claim can be made for the other decision variables.

In the process of searching for the optimum decision variable certain strange attractors were observed. FIGURE 28 through FIGURE 31 show the normalized phase angle versus the frequency of the third and the fourth loops at the instant of the second loop's sampling time. These figures are for two values of the coupling parameter of the first loop, namely $b_1 = 0.1$ and 0.2016 . The coupling parameters for the other loops were; $b_2 = 0.55$, $b_3 = 0.1$, and $b_4 = 0.2016$. It is seen that a well defined strange attractor is observed when the parameter value of the third or fourth loop matches that of the first loop, and the attractor becomes fuzzy when the parameter values are not matched.

FIGURE 32 through FIGURE 41 shows the output voltage of the third and fourth loops at the $n+1$ st sampling time versus the voltage of the second loop at the n -th sampling time. Again, it is seen that it exhibits a well defined strange attractor when the parameter value of the receiving loop matches that of the first loop. This fact could be used to advantage in generating a decision algorithm. It is suspected, however, that the decision algorithm based on these observations would be computationally very extensive and is therefore of little use.

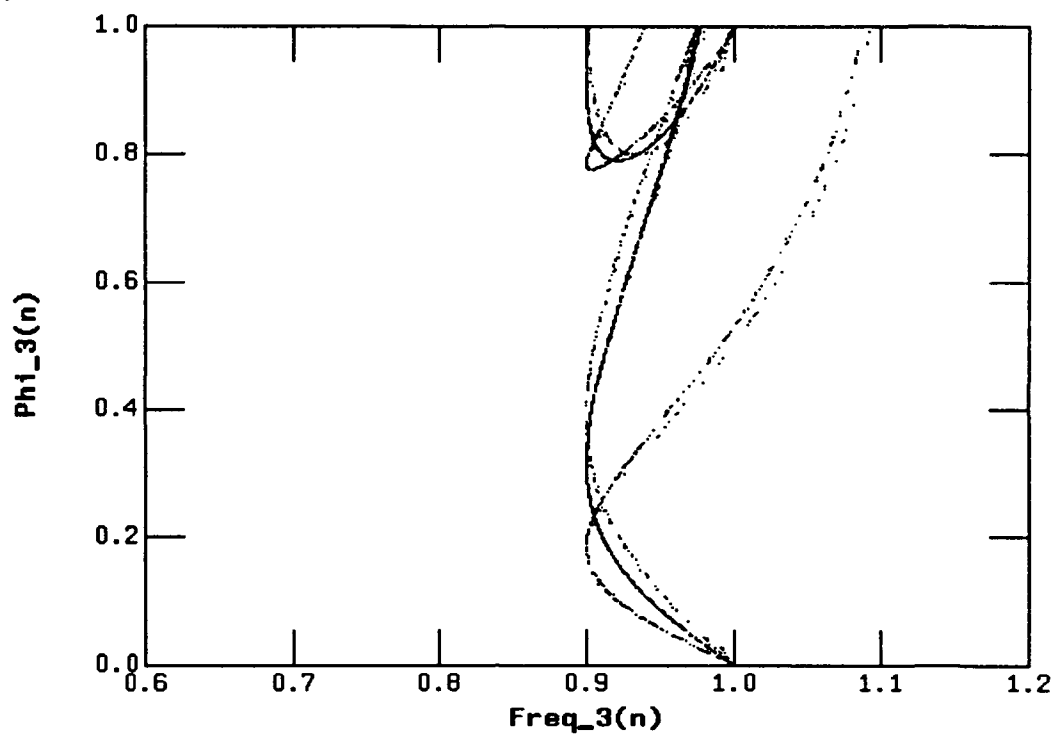


FIGURE 34. Normalized Phase Angle Versus Frequency At the Second Loop Sampling Time For The Third Loop; With $b_1= 0.1$, $b_3=0.1$

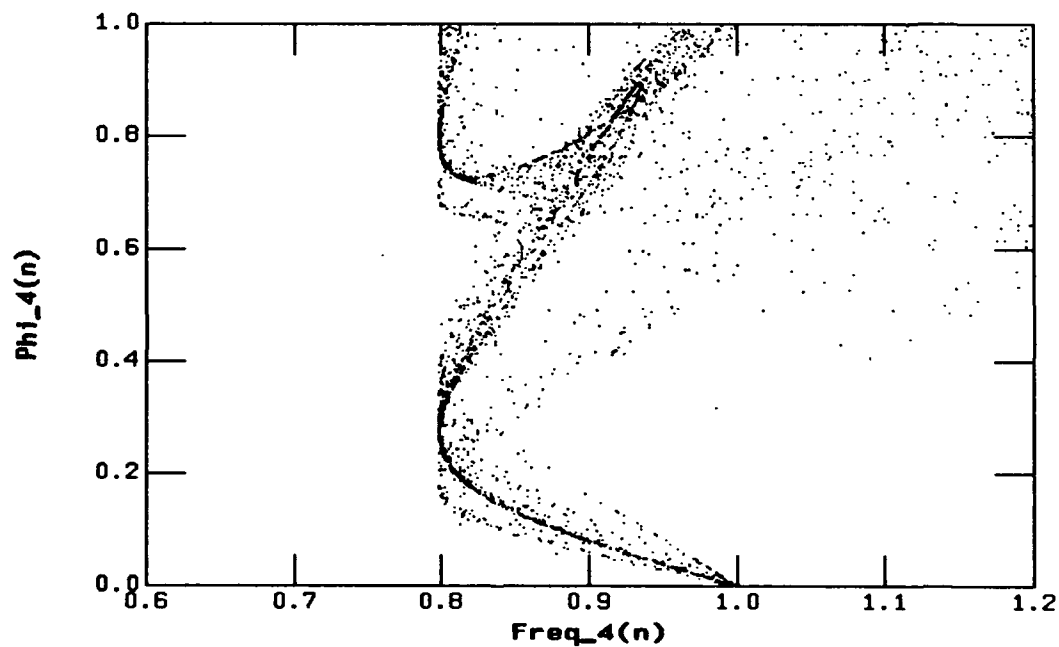


FIGURE 35. Normalized Phase Angle Versus Frequency At the Second Loop Sampling Time For The Fourth Loop With $b_1=0.1$, $b_4=0.2016$

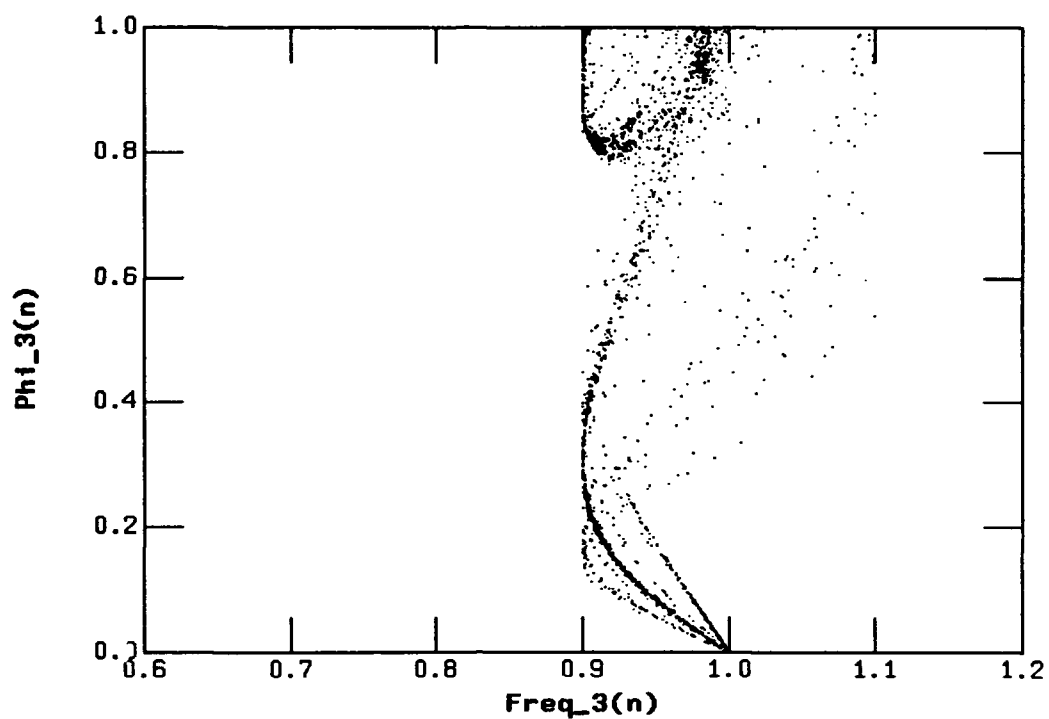


FIGURE 36. Normalized Phase Angle Versus Frequency At the Second Loop Sampling Time For The Third Loop With $b_1= 0.2016$, $b_3=0.1$

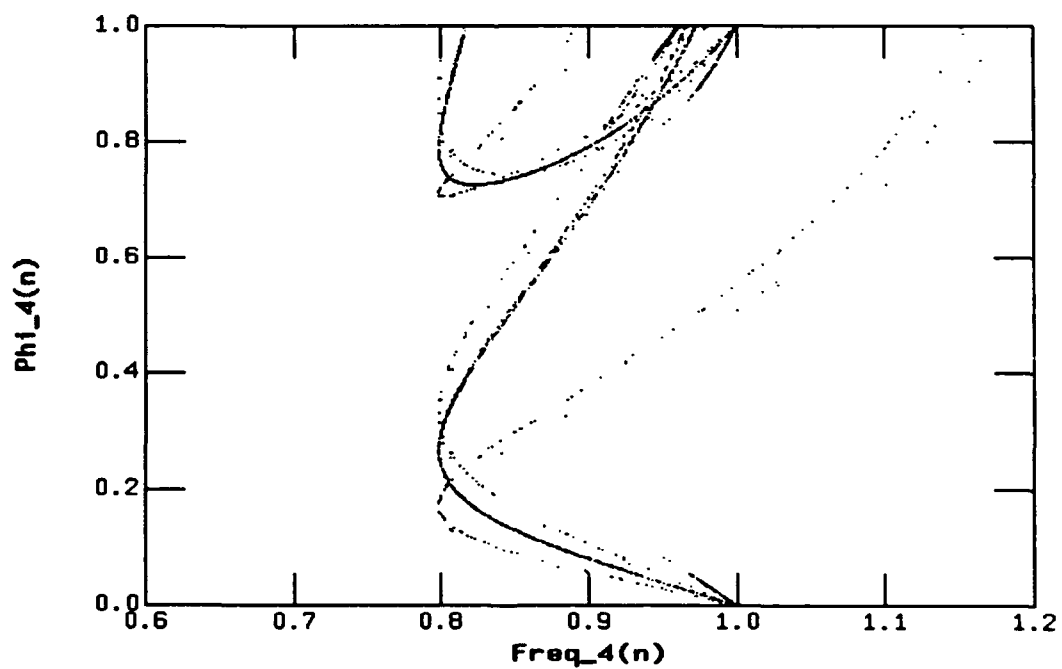


FIGURE 37. Normalized Phase Angle Versus Frequency At the Second Loop Sampling Time For The Fourth Loop With $b_1= 0.2016$, $b_4= 0.2016$

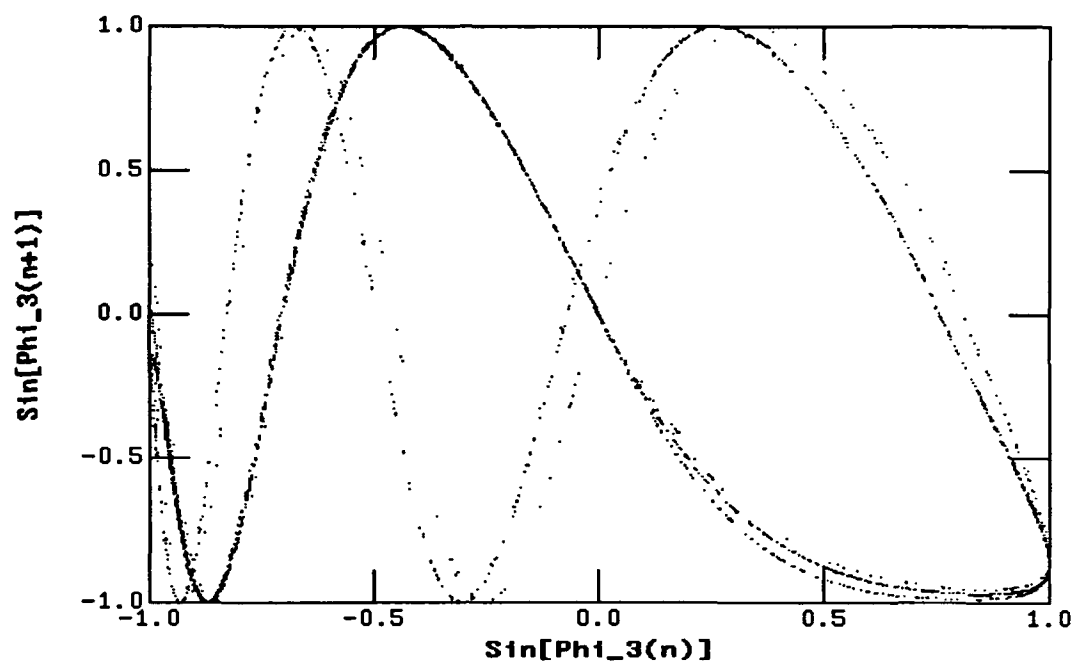


FIGURE 38. The Output Voltage Of The Third Loop At N+First Time Instant Versus The Output Voltage Of The Second Loop At The Nth Time Instant; With $b_1=0.1$, $b_3=0.1$.

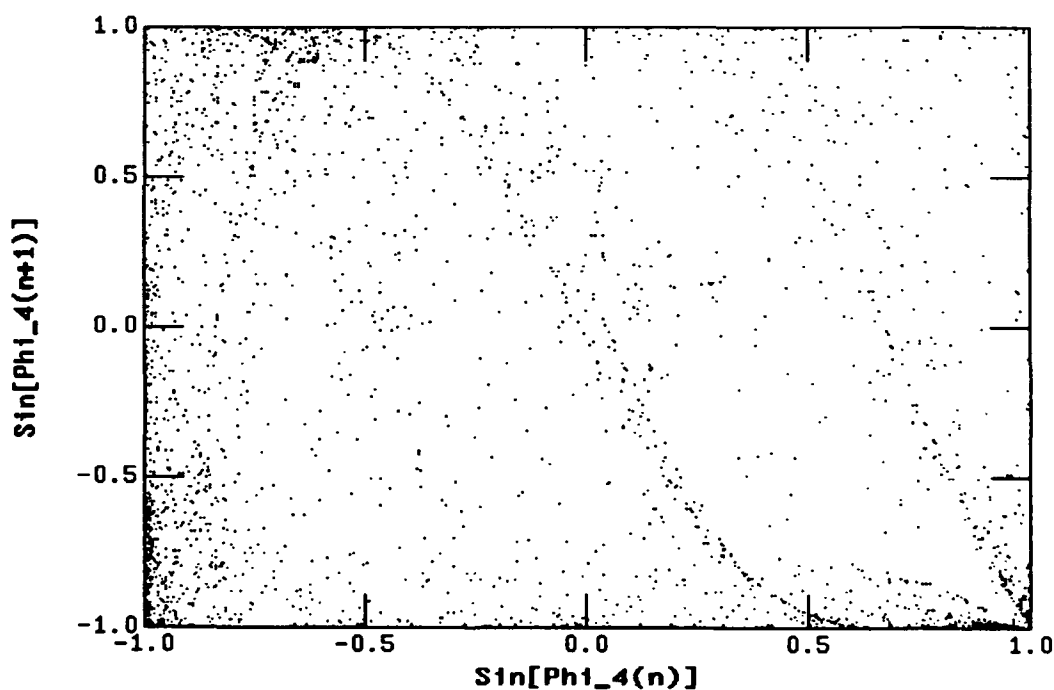


FIGURE 39. The Output Voltage Of The Fourth Loop At N+First Time Instant Versus The Output Voltage Of The, Second Loop At The Nth Time Sampling Instant; With $b_1=0.1$, $b_4=0.2016$

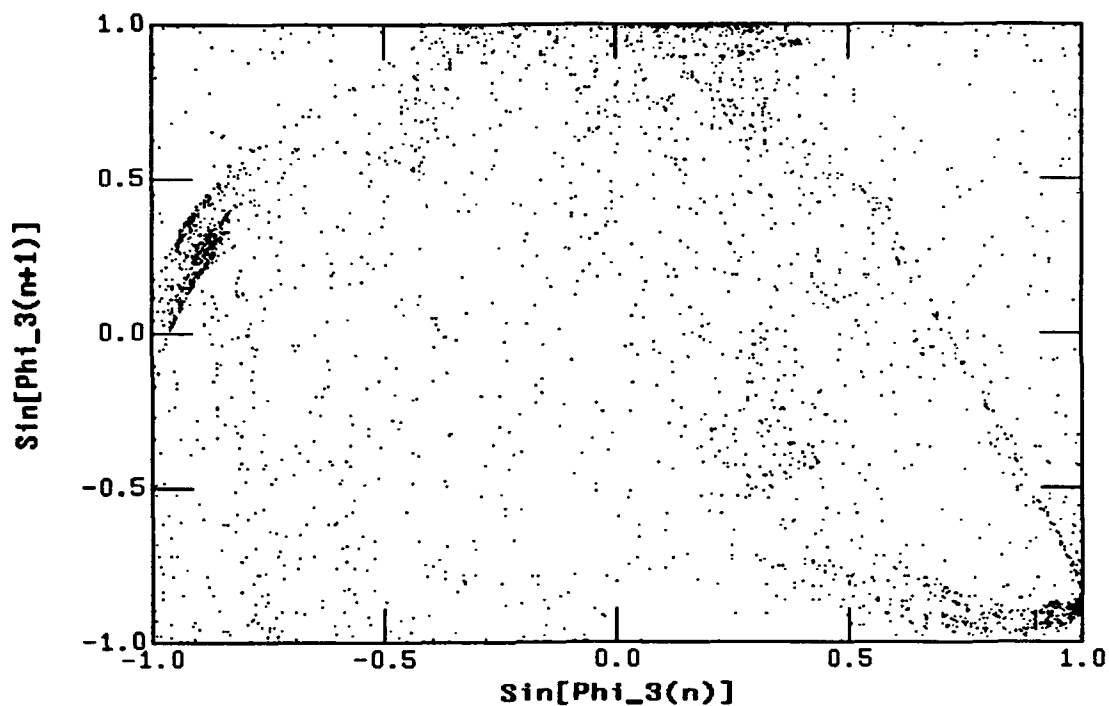


FIGURE 40. The Output Voltage Of The Third Loop At N +First Time Instant Versus The Output Voltage Of The Second Loop At The N th Time Instant; With $b_1=0.2016$, $b_3=0.1$

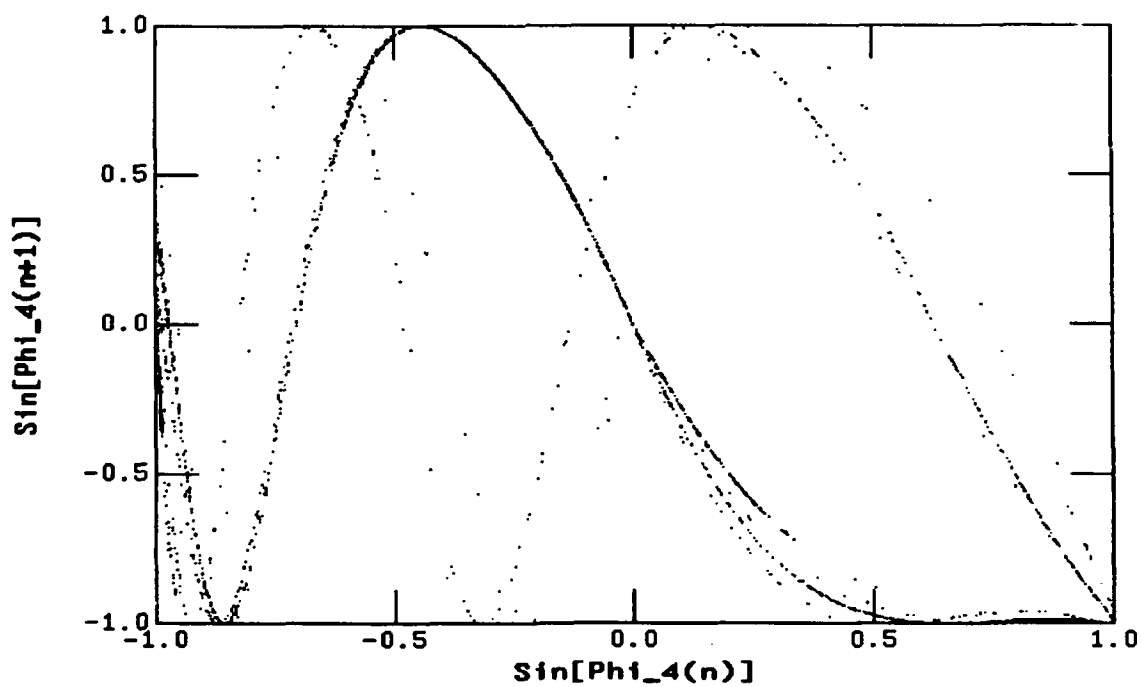


FIGURE 41. The Output Voltage Of The Fourth Loop At N +First Time Instant Versus The Output Voltage Of The, Second Loop At The N th Time Sampling Instant; With $b_1= 0.2016$, $b_4= 0.2016$

3.4.3 Bit Error Probability Versus Input Signal-To-Noise Ratio (SNR).

The bit error probability versus the input signal-to-noise ratio (SNR) for the communication system of FIGURE 33. was generated using a Monte Carlo method. The decision variable based on the second difference of the sampled phase angles of the input signal to the receiver was used. It was found that the coupling coefficients which yielded the lowest bit error probability were: $b_1 = 0.1$ for the 1-bit and 0.2016 for the 0-bit, and $b_2 = 0.55$. The number of samples accumulated = 1,000.

FIGURE 42. is a graph of the bit error probability versus input SNR resulting from the simulation. It is noted that each of the data points is the result of transmitting a sufficient number of random binary digits to obtain fifty (50) erroneously detected bits for the given value of SNR. It can be seen that the bit error probability curve tends to flare out with increasing value of input SNR. This seems to suggest that in order to have a bit error probability in the order of 10^{-6} or lower, the input SNR must be much higher than twenty (20) dB, which is almost one order of magnitude greater than what occurs in practice for BPSK or QPSK signalling systems. Hence, though this digital data transmission system may be considered an LPI communication system its power efficiency is very poor.

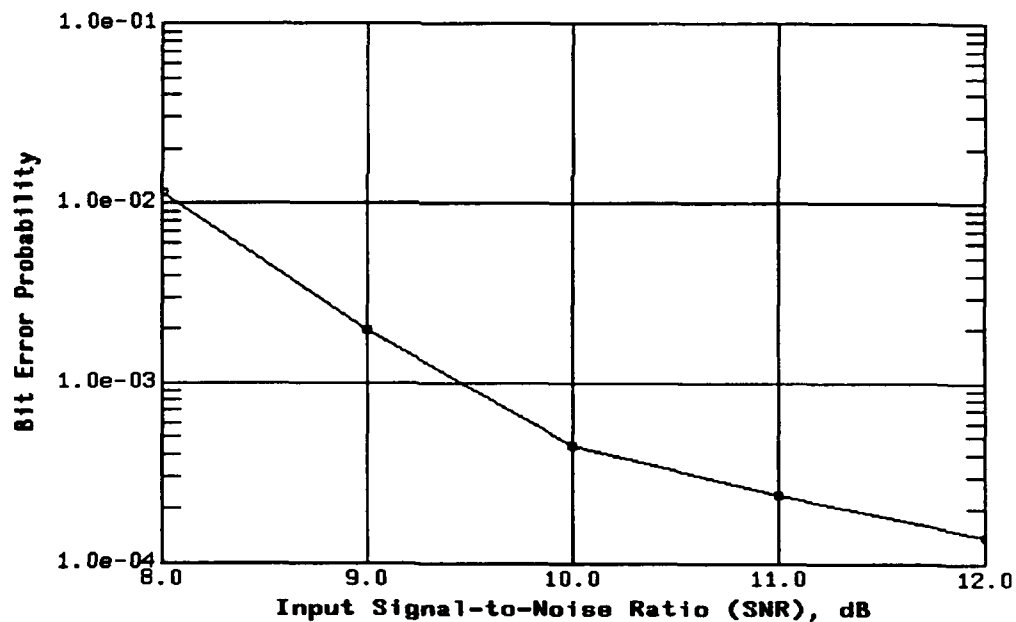


FIGURE 42. Bit Error Probability Vs. Input Signal-to-Noise Ratio (SNR)

In conclusion, it is well to pointed out that the search for the optimal decision variable to achieve minimum bit error probability for a given value of the input SNR, has not been exhaustive, and further investigation is warranted. Also, because the communication channel is band-limited to have a certain frequency response, the effects of filtering distortion on the transmitted signal need to be studied in order to determine how they may impact the detection process.

3.5 Communication System Using Chaotic Signals as Transmitted Symbols

3.5.1 Introduction

In this paper we describe a communication system which uses chaotic signals as the transmitted symbols. The system consists of two coupled DPLLs acting as a transmitter, a modulator, a channel, an additive noise source, a demodulator, and a DPLL acting as a receiver. The coupled loop transmitter operates in a region such that its output is chaotic. The receiver then takes in this chaotic signal and synchronizes to it. It has been shown previously¹ in a simpler system with no channel, noise or modulation that the receiver can synchronize to the transmitter even though the transmitter is operating in a chaotic regime. We extend this idea in an attempt to make a realistic and realizable communications system.

This section is divided into six parts, the first being the introduction. In section 3.5.2 the system under study is described in detail with the reasons why particular choices were made. Section 3.5.3 describes the mathematical models developed to study the system of interest. Section 3.5.4 describes the simulations performed on the system and the results obtained from those simulations. Section 3.5.5 describes the experiments performed on the system and the results of those experiments. Section 3.5.6 contains the conclusions and an assessment of the work under study, including directions for further study.

3.5.2 System Description

The impetus for the present work is given by Vieira et al². In her work she found that two coupled DPLL's operating in a chaotic regime could synchronize with a third loop. In the coupled loop "transmitter" one of the loops operates in an unstable mode and the other in a stable mode, much as in the idea developed by Pecora³. But in this case instead of a single chaotic circuit being subdivided into its stable and unstable components she had two circuits both of which, with the proper forcing function⁴, can operate in a chaotic mode independently. The receiver then, mimicking the stable loop in the transmitter, synchronizes with the transmitter. FIGURE 43. is a block diagram of the simple system given by Vieira. In this system V_1 and V_3 are equal even though the system is operating in a chaotic regime.

It should be made clear at this point that the fact that the transmitter and receiver are composed of phase locked loops is purely incidental, other chaotic circuits which can be subdivide into stable and unstable subsets could also have been used. The DPLL's are not operating in a regime where they operate as standard DPLL's. Instead as stated previously the PLL's in the transmitter together compose a single chaotic circuit, with stable and unstable subsets. The purpose of the receiver is then to mimic the stable portion of the transmitter, not to lock onto a specific frequency as with carrier recovery nor to demodulate a signal such as FM.

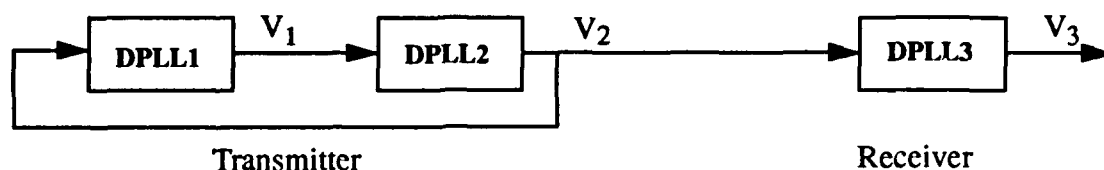


FIGURE 43. Simple Synchronization System With No Channel

A full description of the coupled loop system is given by Vieira et al². A short description will be given here. Each DPLL consists of a voltage controlled oscillator (VCO), and a sample and hold (SH) amplifier. During operation, the VCO signals the SH to take a sample, $v_{in}(t_i)$, at the sampling time t_i . For standard operation the sampled value is used to control the sampling frequency of the VCO in such a way so as to decrease the phase difference between the incoming signal and the VCO output. As a result, for a range of parameters, there is a possibility of locked behavior when the VCO frequency adjusts itself to the input frequency and locks to its phase, hence continually sampling at the same point of the input periodic signal. Due to non-linearities in the system, for certain parameter values, orbits with high period, quasiperiodic and chaotic behavior may also appear in a single DPLL⁴ which is the behavior of interest for this application. The block diagram of a single first order DPLL is given in FIGURE 44. . The coupled loop system is then created by connecting two loops together such that the output of one is the input of the other and vice versa. The input to the receiver is the output of the unstable loop in the transmitter.

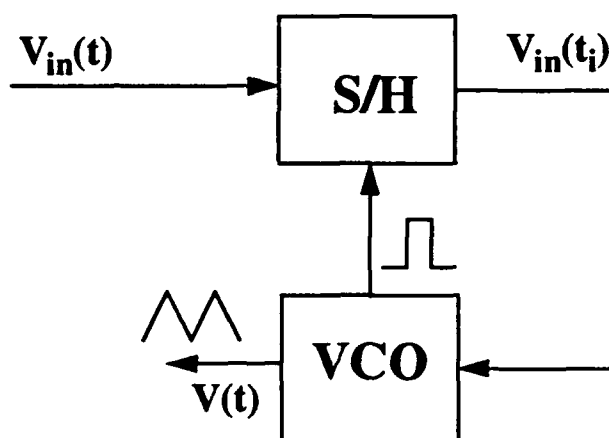


FIGURE 44. Block Diagram of single DPLL

Unfortunately the simple coupled loop system is not adequate to be a communication system in and of itself. There is no modulation of data and channel effects are ignored. Another problem is that synchronization is blind in the simple system in the sense that

even if V_3 is equal to V_1 the receiver would not know. This requires one of two things to happen in a realistic communication system. Either V_1 must be transmitted as a reference or some algorithm must be developed that can tell if the receiver is in lock. This section will concentrate on the transmitted reference scheme. Work is also being performed on the latter method and will be presented elsewhere (see section 3.4 of this report).

The transmitted reference system is composed of six main parts; transmitter, modulator, channel, additive noise source, demodulator and receiver. FIGURE 45. is a block diagram of the communication system.

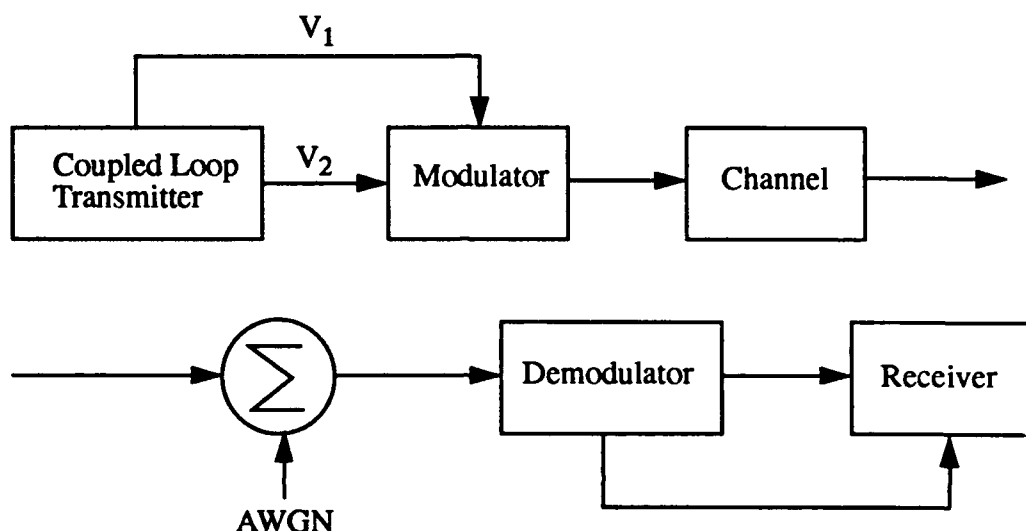


FIGURE 45. Block Diagram of General Communication System Using Coupled Loop Transmitter.

The coupled DPLLs act as the transmitter. Data is transmitted by changing the parameter values of the DPLLs, (more about this later). Since both V_1 and V_2 are to be transmitted they must be multiplexed in some manner. There are two obvious multiplexing schemes to choose from, Frequency Division Multiplexing (FDM) and Quadrature Multiplexing (QM).

In frequency division multiplexing the signals are mixed according to eqn(44). Let $s(t)$ be the modulated signal.

$$s(t) = V_1(t) \cos(\omega_1 t + \Theta_1) + V_2(t) \cos(\omega_2 t + \Theta_2) \quad (44)$$

Where ω_1 and ω_2 are the carriers of V_1 and V_2 respectively. The bandwidths, B_1 and B_2 , of V_1 and V_2 , and the carrier frequencies obey the relations,

$$\omega_2 - \omega_1 > \frac{B_1 + B_2}{2} \quad \text{and, } \omega_2 > \omega_1 \gg B_1 \approx B_2. \quad (45)$$

These requirements insure that the spectra of V_1 and V_2 will not overlap. Also note that the bandwidth B_s of $s(t)$ is governed by the relation $B_s > B_1 + B_2$.

In quadrature multiplexing the signals are mixed according to eqn (46).

$$s(t) = V_1(t) \cos(\omega t + \Theta) + V_2(t) \sin(\omega t + \Theta) \quad (46)$$

Where ω is the carrier frequency which obeys the relation $\omega \gg B_1 \approx B_2$ and the Bandwidth of $s(t)$ is given by $B_s \approx B_1 \approx B_2$.

The use of quadrature multiplexing was chosen over FDM because FDM would take twice as much bandwidth to perform the same job as in QM. Quadrature multiplexing also makes it less apparent to the casual observer that communication is taking place. This can be seen by a comparison between eqn(44)and eqn(46). Assume that the spectrum of V_2 is held constant and the spectrum of V_1 changes slightly as data is modulated onto it. In FDM all changes in the spectrum are readily apparent in the frequency band associated with the changing signal. In QM the two signals occupy the same frequency band thus a change in one is partially masked by the other. In an actual system V_2 will not remain constant but changes in the spectrum are still less apparent in QM than they are in FDM. A block diagram of a quadrature multiplexer is given in FIGURE 46.. The D.C. portion of V_1 and V_2 must be eliminated before the signals are mixed with the carrier or else the transmitted signal $s(t)$ will not be suppressed carrier.

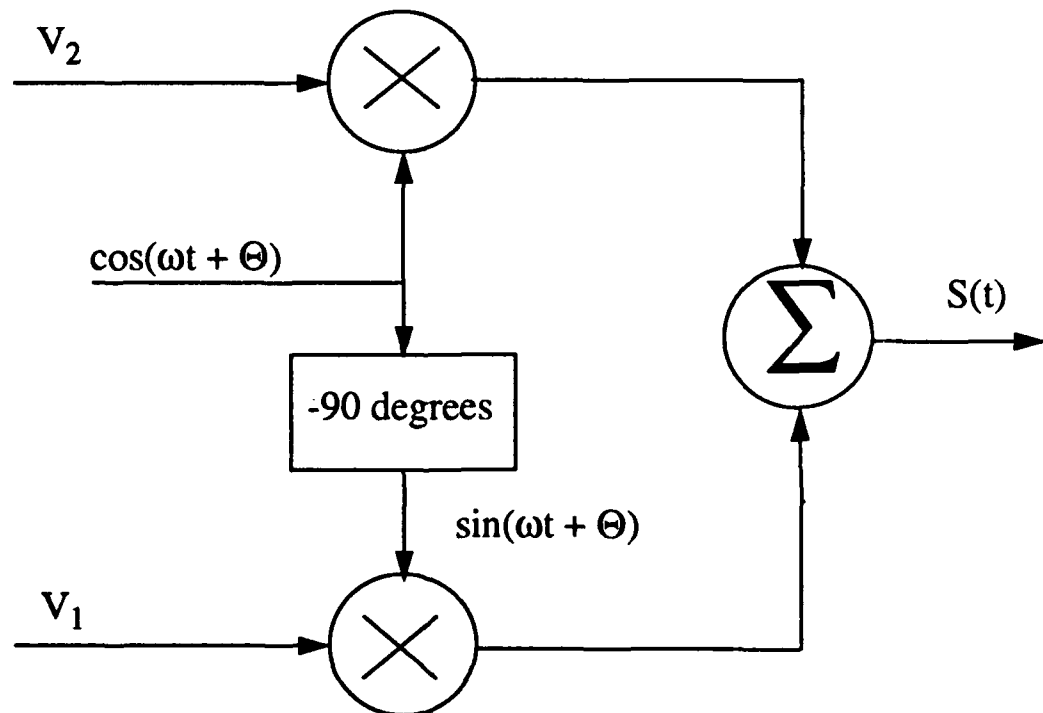


FIGURE 46. Block diagram of Quadrature Multiplexer.

For the purposes of this study the channel will be modeled as an AWGN channel only. Proakis⁶ gives an excellent and lengthy description of this type of channel, therefore it will not be repeated here.

The demodulator is a standard quadrature demodulator. Since the transmitted signal, $s(t)$, is suppressed carrier the first thing that must be done is to recover the carrier. This is done by raising $s(t)$ to the fourth power and passing this through a narrow band pass filter at around four times the carrier frequency. A phase locked loop is then used to recover the exact frequency and phase of this signal. Note that this PLL is not the same as the ones used in the transmitter and receiver, but instead a second order analog PLL. The recovered frequency is then divided by four and used as the recovered carrier. FIGURE 47 is the block diagram of the quadrature demodulator. The input to the demodulator is assumed to be a signal plus white Gaussian noise. In the demodulator the signal is split into two paths, one gets multiplied by a cosine and the other by a sine. These signals are then passed through low pass filters to eliminate the double frequency components. This assumes that carrier recovery was done perfectly. The low pass filtering causes a problem. Since the receiver must be identical to a stable portion of the transmitter, all parameters of the receiver must match the parameters of the stable portion of the transmitter. Two of these parameters are the amplitude and offset voltage of the input to the DPLL. Clearly after passing through the low pass filters in the demodulators the signal will not have the same amplitude as it had on the transmitting side. This problem is compounded by the fact that because the low pass filters in the demodulator are not ideal the received signal's amplitude will also vary with frequency, as the frequency goes up attenuation increases. Since chaotic signals are wide band this is a very detrimental effect. A partial solution to the problem is found in the addition of an automatic gain control device. Although this device will not correct the problem of amplitudes varying with frequency it will make the average amplitude occur at it's proper value. There is also the problem that the D.C. offset of the receiver input must be identical to the D.C. offset of the transmitter output. This value must be known a-priori because no D.C. is allowed to be modulated.

The receiver consists of a single DPLL mimicking the stable DPLL in the transmitter. The input to the DPLL, $r(t)$, is,

$$r(t) = V_2(t) + n(t) \cos(\omega t + \Theta). \quad (47)$$

The output of the receiver is then compared to the transmitted reference, $q(t)$, which is,

$$q(t) = V_1(t) + n(t) \sin(\omega t + \Theta). \quad (48)$$

The output of the receiver, $o(t)$, is given by,

$$o(t) = \hat{V}'_1(t) + n_o(t). \quad (49)$$

where $\hat{V}'_1(t)$ is a distorted version of the transmitted reference and $n_o(t)$ is the noise output of the receiver including all inter-modulations of the signal and noise input. FIGURE 48. is a block diagram of the receiver.

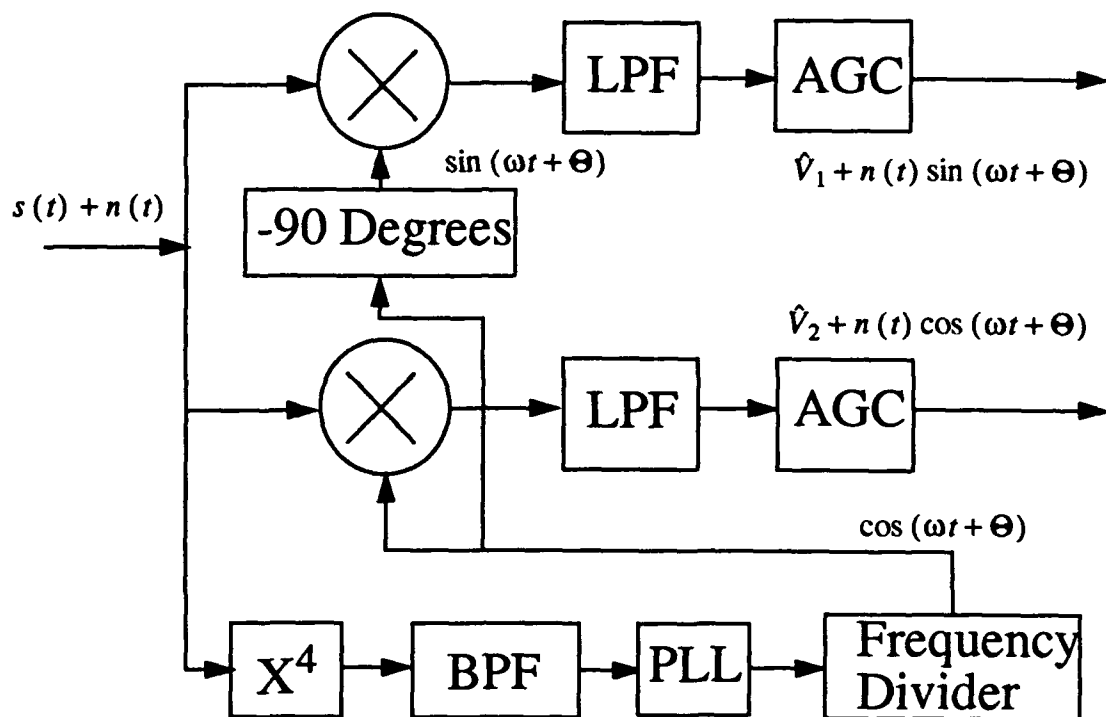


FIGURE 47. Block Diagram of the Quadrature Demodulator.

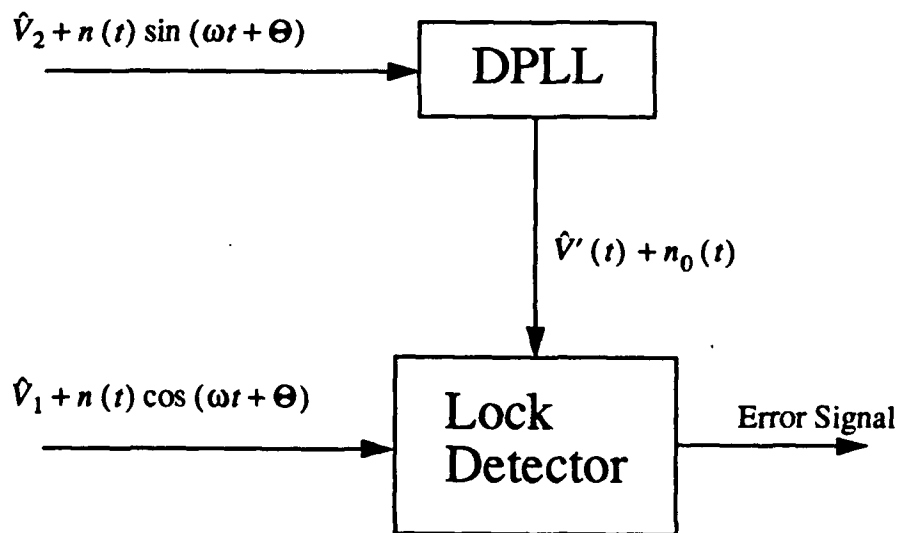


FIGURE 48. Block Diagram of Receiver

3.5.3 Mathematical Models

The mathematical models used to describe this system are presented here. The algorithm given by Vieira¹ is used to iterate through the equations governing the DPLL's. The algorithm will be repeated here for completeness.

Given the frequencies $\omega_1, \omega_2, \dots, \omega_n$ and phases $\theta_1, \theta_2, \dots, \theta_n$ of the VCO's at $t = 0$ then:

1. Initialization: Find what should have been the last sampling time t_i and the next sampling time t'_i for all loops ($i = 1, 2, \dots, n$).

$$t_i = \frac{-\theta_i}{\omega_i}, \quad (50)$$

$$t'_i = \frac{2\pi - \theta_i}{\omega_i}. \quad (51)$$

2. Search over the DPLL's to find the loop l with the smallest time for the next sampling; that is, find l such that

$$t'_l = \text{smaller}(t'_i). \quad (52)$$

3. Calculate the input sample value of the loop that samples.

$$v_i(t'_l) = \Lambda(\phi_i), \quad (53)$$

where

$$\phi(i) = \omega_i(t'_l - t_i), \quad (54)$$

and $\Lambda()$ is the triangle function for the VCO output.

4. Update the frequency of the loop l according to,

$$\omega'_l = \omega_0 + b_l v(t'_l). \quad (55)$$

5. Set $t_l = t'_l$ and $t'_l = t_l + 2\pi / (\omega'_l)$. Go to step 2.

Since the DPLL's are nonuniformly sampling, and filters are present in the system which require uniform spaced sample values, an algorithm for converting from the nonuniformly sampling time domain to uniformly sampled time domain was developed. The algorithm works as follows.

1. Get the start time, t_l , and the stop time, t'_l , from the algorithm above.
2. Calculate the number of steps necessary to traverse the time span.

$$N = \frac{t_l' - t_l}{t_s} + 1 \quad (56)$$

Where t_s is the step size and N is the number of steps.

3. Calculate the actual uniformly spaced time values.

$$T_j = t_l + jt_s, \text{ for } j = 1, 2, \dots, N \quad (57)$$

Note that the relationship between the final time and the stop time.

$$t_l' \leq T_N \leq t_l' + t_s. \quad (58)$$

4. Calculate the actual values of the state variables of interest for all T_j .

After passing through the filters the signals must be converted back into the nonuniformly sampled time domain. This is accomplished by performing a linear first order interpolation on the state variable of interest. Let $x(t_l')$ represent the state variable's value at the nonuniform sampling time, and let $x(T_N)$ and $x(T_{N-1})$ represent the value of the state variable at the last and second to last uniform sampling point respectively. The equation for finding $x(t_l')$ is given by,

$$x(t_l') = x(T_{N-1}) + \frac{(x(T_N) - x(T_{N-1})))}{T_N - T_{N-1}} \times (t_l' - T_{N-1}) \quad (59)$$

All filters in this system are modelled in the Z domain. Thus they are implemented with difference equations. (The filters were designed in the laplace transform domain and converted to the Z domain by means of a bilinear transformation.)

3.5.4 Simulations Performed

A description of the software written will be given first. The software produces a simulation of the system which is described in the section 3.5.2; it does this by using the algorithms described above and by calculating the state variables (equations given in section 3.5.3) at the appropriate times. The program was written in C on a Sun 3/60 unix based workstation. The total number of lines of code written is 1,367.

The program is set up as follows. It consists of eight source files which are compiled together to create one executable file. Along with these eight source files there is one input file. The input file consists of all of the parameters in system that one would wish to change while investigating the system. The input file also contains the control statements for the output. The user indicates which signals are to be output to a file and how much of the signal is going to be stored. There are a total of fifteen possible output files. Among the variables that are able to be stored are; the outputs of the transmitter, the outputs of the modulator, the output of the noise source, the outputs of the demodulator before and after

the AGC's, and the output of the receiver. The output is stored in a two column format with time in the first column and the state variable in the second column. These outputs may then either be plotted or some post-processing performed. The post-processing includes fourier transformations and the determination of Lyapunov exponents.

There were several steps in the simulation process. First, the coupled loop system, as shown in FIGURE 43., with no channel, modulation, or noise was simulated. As expected, synchronization was obtained between V_1 and V_3 even though the coupled DPPLs were operating in a chaotic regime. Synchronization is shown in FIGURE 49. while FIGURE 51. shows the spectrum of the chaotic signal. Next the outputs of the transmitter were transformed into the uniformly sampled time domain and then back into the nonuniformly sampled time domain before entering the receiver. This has the effect of adding on a small amount of noise to the received signal. Once again synchronization was obtained between V_1 and V_3 . This is shown in FIGURE 50.

Finally the modulator and demodulator were added into the system, but, carrier recovery was not performed. In this case synchronization was not obtained. The reason was because the low pass filters smoothed the triangle wave and, as described previously, amplitude modulated it also. Thus the tips of the triangle were clipped and the peaks were not of the same height. FIGURE 52. is a graph of the input to the modulator and the output of the demodulator. It also shows the output of the demodulator after it has passed through an automatic gain control device. The receiver DPPL's output, now with the distorted input, did not match the transmitted reference, see FIGURE 54..

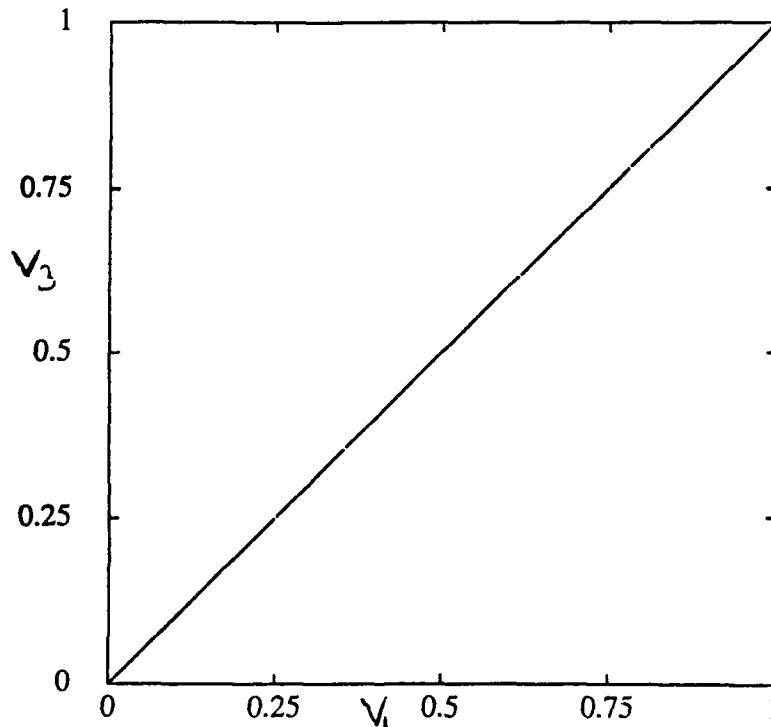


FIGURE 49. Synchronization of Simple Coupled System

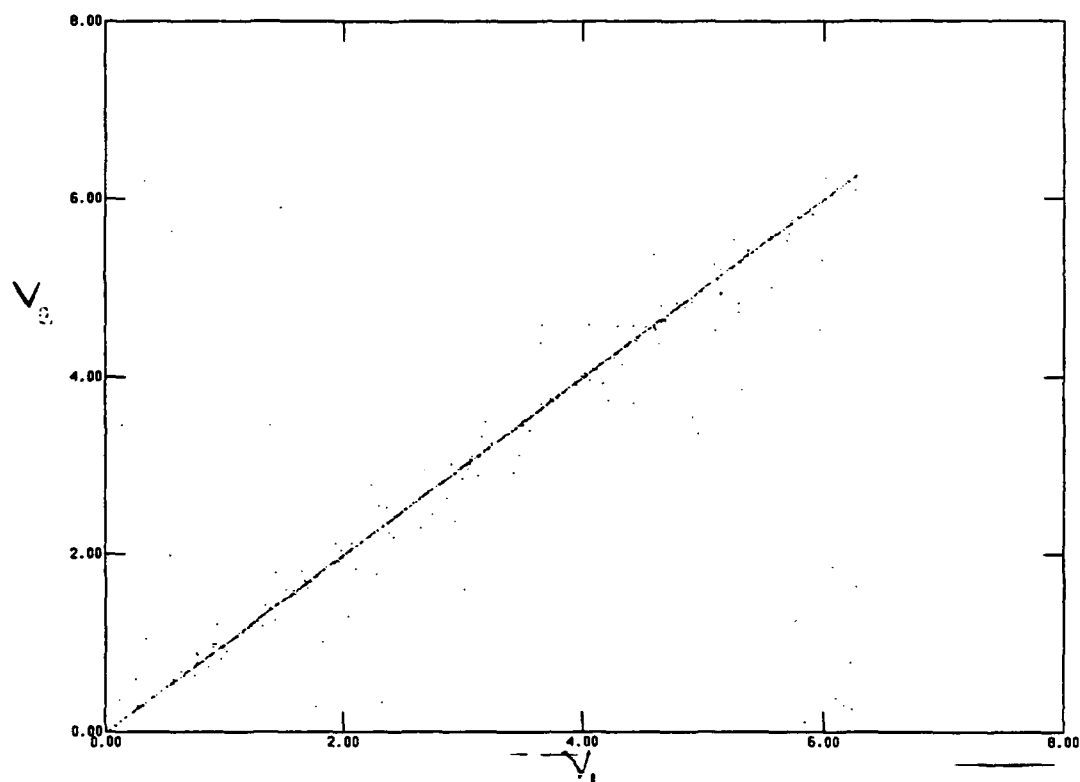


FIGURE 50. Synchronization when Domains are changed

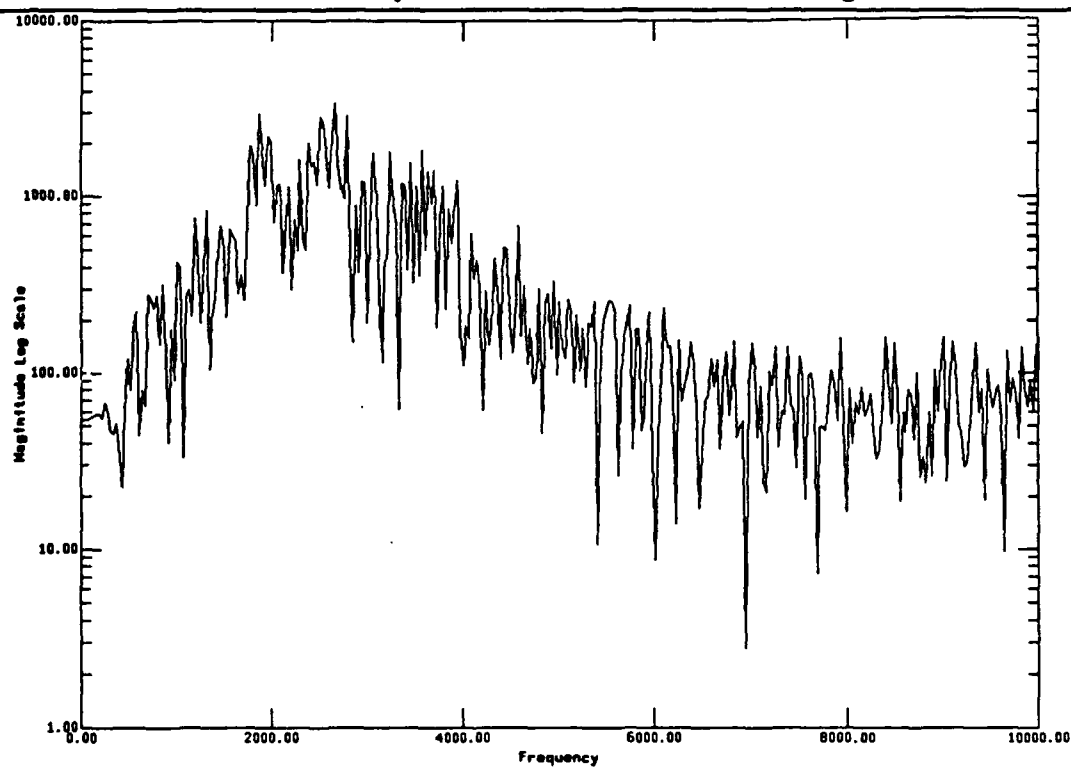


FIGURE 51. Spectrum of Transmitted Signal When System is Operating in a Chaotic Mode.

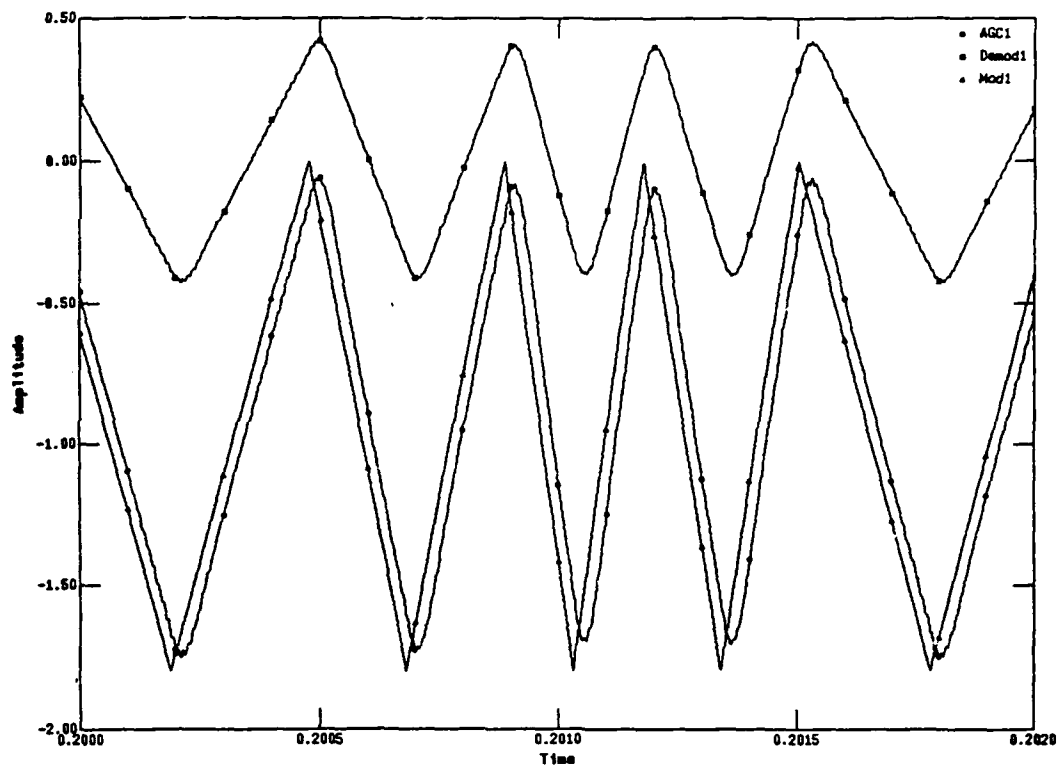


FIGURE 52. Input and Output of Channel and Output of AGC

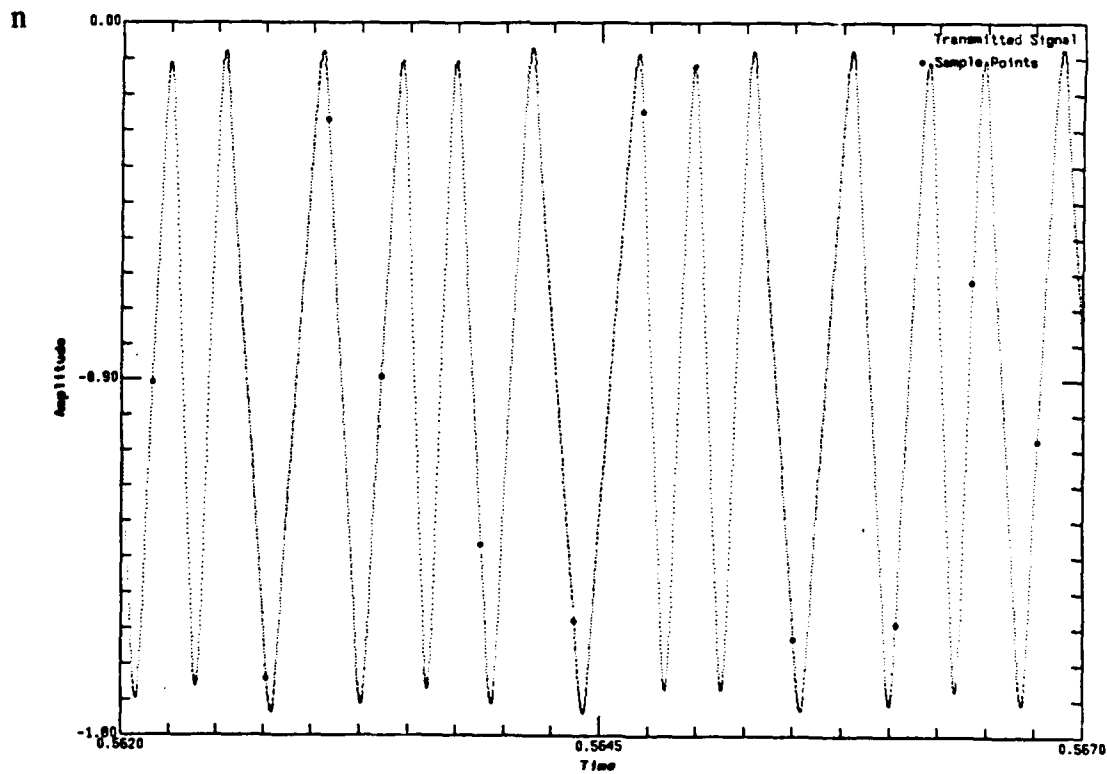


FIGURE 53. Distorted Input to the Receiver

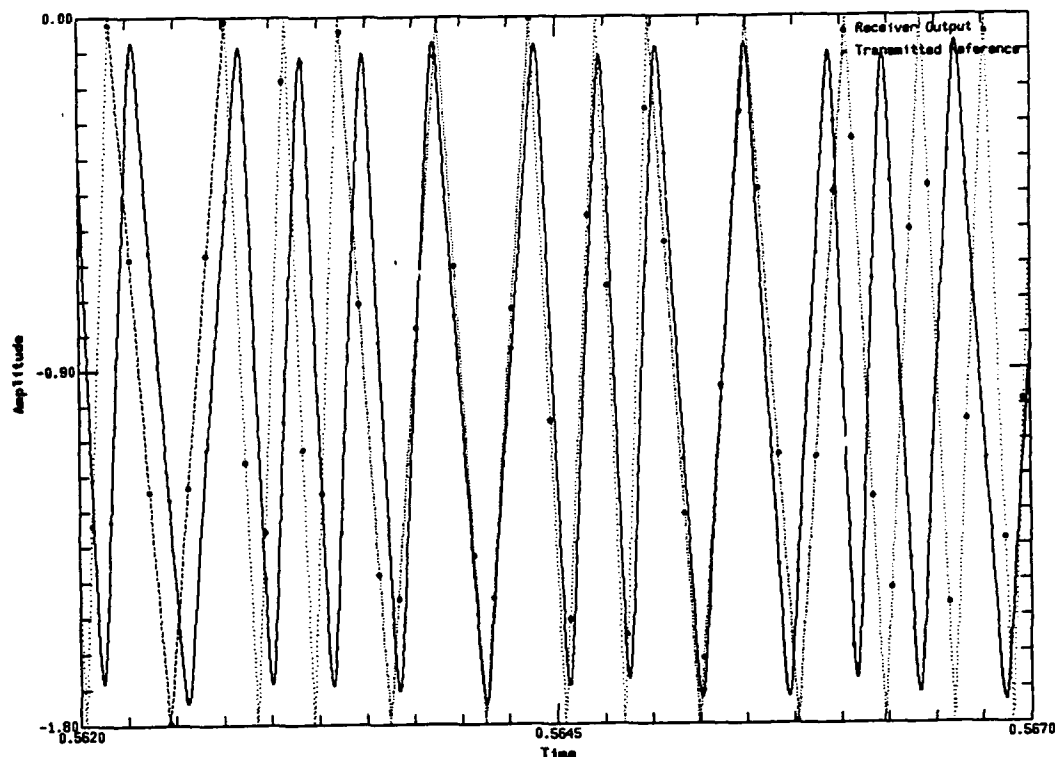


FIGURE 54. Receiver Output Versus Transmitted Reference

3.5.5 Experiments Performed

The experiments performed so far are all on the simple coupled loop system. That is two DPLL's in the transmitter and one in the receiver, as shown in FIGURE 43.. The schematic of a single DPLL is given in FIGURE 55.. The circuit⁵ is composed of two main parts: (1) the sampler and associated support circuitry and (2) the VCO and associated circuitry. For the sampler a National Semiconductor LF398 Monolithic Sample and Hold circuit is used. An 0.001 μF polystyrene capacitor is used for its low dielectric loss properties as the hold capacitor. The sample time is set by a 74LS123 re-triggerable monostable multivibrator. The pulse width of the multivibrator is set with $R_{\text{ext}} = 20 \text{ k}\Omega$ and $C_{\text{ext}} = 680 \text{ pF}$ which gives a predicted pulse duration of about $6.7 \mu\text{s}$ and a measured pulse duration of about $6.0 \mu\text{s}$. The maximum frequency of the input signal is about 4kHz. Therefore, our sampling duration is about 2.4% of the signal period in the worst case and less than 2% on average. Hence, our sampling error should be much less than 2%.

For the VCO a National Semiconductor LM566 Voltage Controlled Oscillator integrated circuit is used. The frequency of the VCO is given approximately by the formula

$$f = \frac{2.4(V^+ - v_5)}{R_1 C_1 V^+} \quad (60)$$

where $V^+ = 5V$, v_5 is the control voltage input (the voltage on pin 5 minus the voltage on pin 1 of the integrated circuit), $R_1 = 10k\Omega$ and $C_1 = 0.022\mu F$.

Due to the relatively loose tolerances of R_1 and C_1 and the temperature dependence of these components, equation (60) is useful primarily for design purposes. The center frequency and gain of such a DPLL, which obeys $f = f_0 + bv$, with v being referenced to zero, were obtained from a linear least squares fit of the data, and it was found that $f_0 = 5259.1\text{Hz}$ and $b = 1217.4\text{Hz/V}$ for the voltage range we use. The output of the VCO has an amplitude of 0.9 V and a D.C. offset of -0.9 V. To use this VCO in a DPLL it is necessary to add D.C. offset voltage either to the input signal of the sampler or to the output of the sampler so that the input signal to the VCO will be in the proper voltage range. The operational amplifier circuit shown in figure seven is used to adjust the offset voltage. A hard limiter LM311 with a reference of -0.9 V was included at the triangle wave output of the VCO to cause sampling at the zero crossing, as opposed to sampling at the peak, as in the case of the circuit studied in Ref. 4.

Bernstein⁴ has shown that a single DPLL can be forced into chaotic regime with a sinusoidal input. In this experiment instead of a sinusoidal input to the DPLL we couple two loops together so that the output of one is the input to the other. The parameter used to control the behavior of the experimental system is the input offset voltage of the VCO. We experimentally verify that this circuit can operate in a chaotic regime. The verification of this is not stringent. We do not measure Lyapunov exponents of any of the experimental signals. Instead we look at the spectrum of the output of one of the loops. When the spectrum of the loops output is observed to be wide and noise like in nature we consider the loop to be operating in a chaotic regime. As opposed to this when operating in a periodic regime one sees only a fundamental and few harmonics on the spectrum analyzer. Other more complicated spectrums also emerge that are clearly not chaotic. FIGURE 56. is the spectrum of the transmitted signal when the system is operating in a chaotic mode. While is the spectrum of the transmitted signal when operating in a period two mode, i.e. the transmitted signal jumps back and forth between two distinct periods. The case when the signal is periodic is not shown

While operating in a chaotic regime, synchronization was obtained as shown in FIGURE 58.. The output voltage of the stable DPLL in the transmitter (x axis) is plotted versus the output voltage of the receiver (y axis)

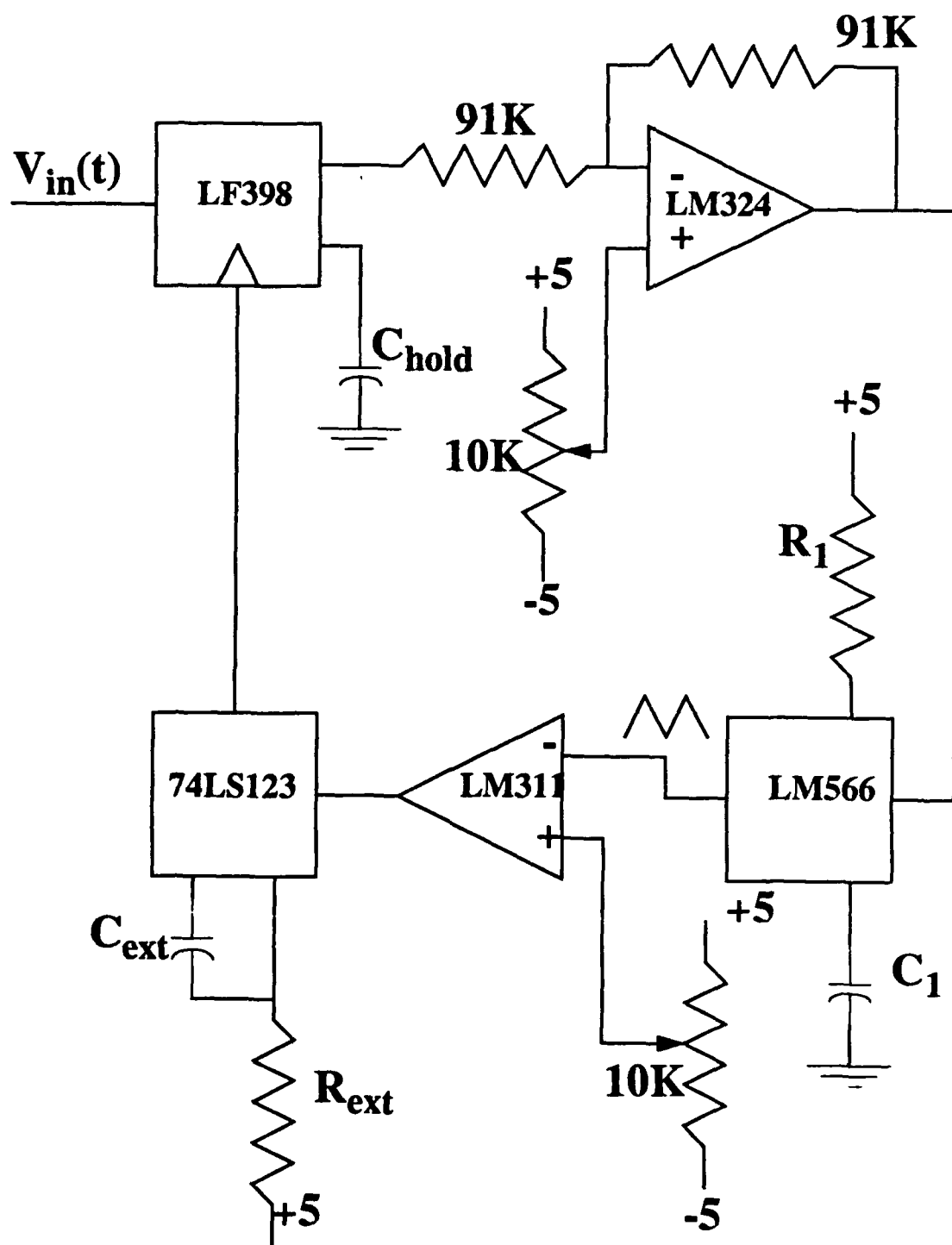


FIGURE 55. Schematic Of A Single DPLL

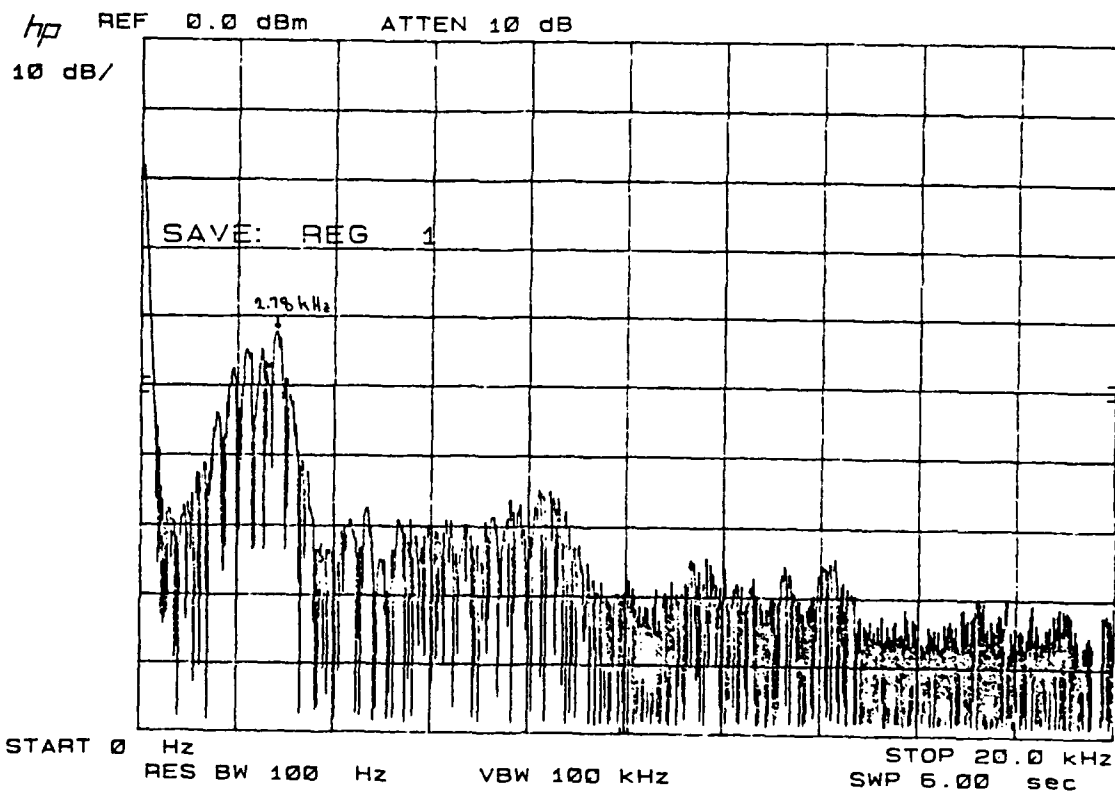


FIGURE 56. Spectrum of Chaotic Signal for Experimental Circuit.

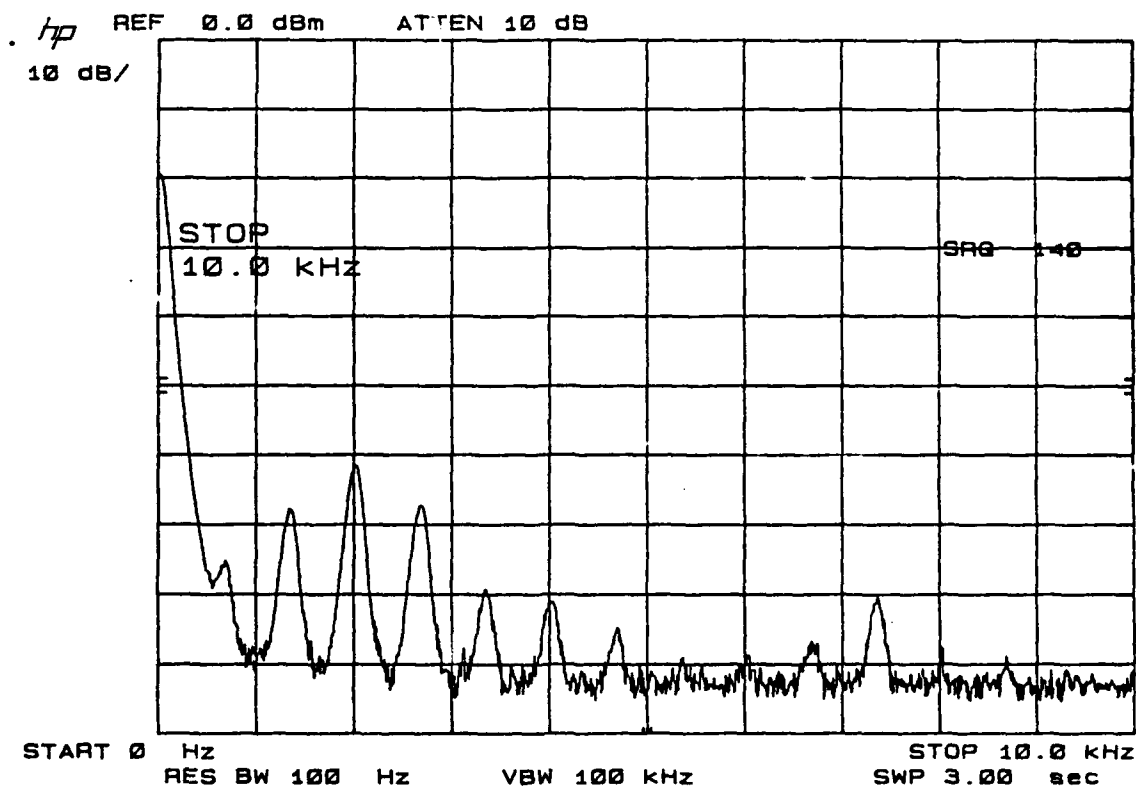


FIGURE 57. Spectrum of Signal in Period Doubling Mode

CH1 100mV~ A 200μs -46.9mV? VERT
CH2 500mV~

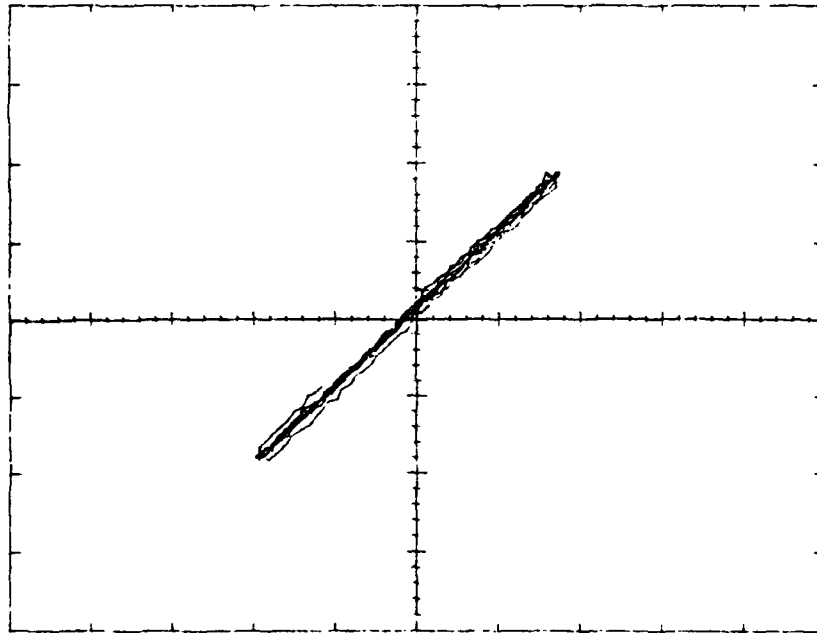


FIGURE 58. Experimental Verification of Synchronization While Operating in a Chaotic Regime

3.5.6 Conclusions

The results from the experimental circuits are encouraging. For the coupled loop system with no channel, modulation, or noise, synchronization is obtained. This is promising because no particular care was taken in assuring that all parts in the receiver and transmitter were matched. The resistors used have a tolerance of 1% and the capacitors a tolerance of 5%. The integrated circuits used were all of the low grade commercial type, not the high A grade commercial or military versions. So clearly the stable DPLL in the transmitter and the DPLL in the receiver will not exactly match.

The results from the simulations are also encouraging. As mentioned in the simulations section synchronization is not obtained between the output of the receiver and the transmitted reference. This problem is not as severe as it may sound. The solution is two-fold. First abandon the use of the triangle wave output VCO's and use sine wave output VCO's instead. This would help solve the problem of the low pass filters in the demodulator smoothing out the signal. The LPF's cut out the harmonics of the triangle wave but with sine waves this should not be a problem. Changing to sine wave output VCO's would also mean that a new circuit has to be made or the present one modified. Second an amplifier should be added directly after the LPF's in the demodulator. The

amplifier would have unity gain for all frequencies except for those in the passband of the LPF's. There the amplifier should have a gain of one over the gain of the LPF. In this way all frequencies entering the AGC will have approximately the same amplitude.

The lock detector in the receiver also must be designed so that data may be transmitted. First a slight change to the receiver must be introduced. The receiver must now consist of two DPLL's, one matched to receive a "1" and the other matched to receive a "0". To clarify this; the transmitter will send bits at a given bit rate by changing the input offset voltage of the VCO in the stable DPLL between two values. The two DPLL's in the receiver each are matched to one of these values. The lock detector will operate by finding the difference in energy between the output of each DPLL and the transmitted reference. These two values will then be subtracted to obtain the decision variable. The sign of the decision variable will determine which bit was sent. FIGURE 59. illustrates this scheme. After the system is operating properly with the modulator and lock detector in place, the noise source will be introduced.

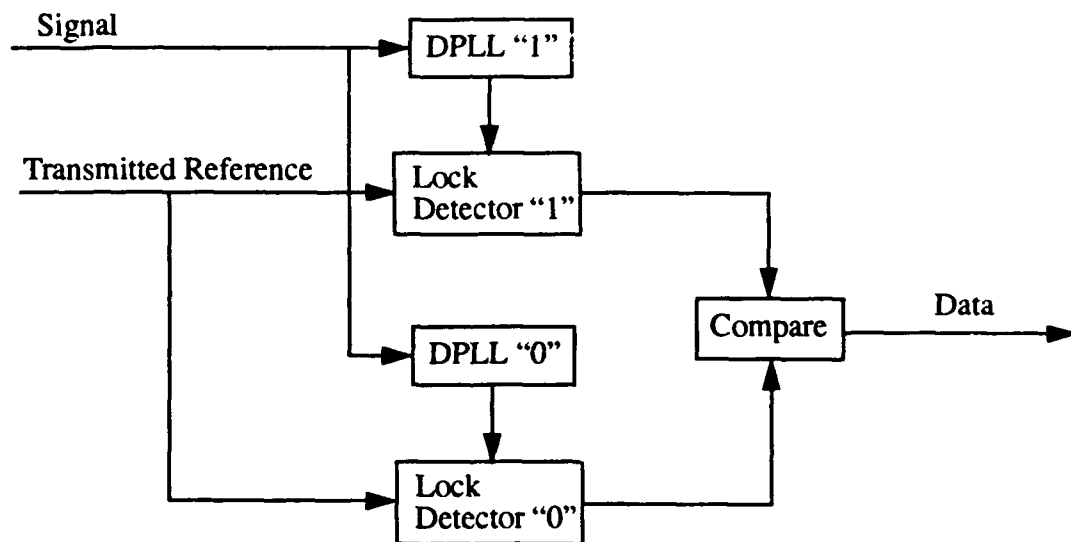


FIGURE 59. New Bit Detection Scheme

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2. M. de Sousa Vieira, A. J. Lichtenberg, and M.A. Lieberman, to appear in International Journal of Bifurcation and Chaos. and sections 3.1 and 3.2 of this report.
3. L.M. Pecora and T.L. Carroll, Phys. Rev Lett. **64** (1990) 821.
4. G.M. Bernstein, Ph.D. Thesis University of California, Berkeley, 1988.
5. J. Gullicksen, M. de Sousa Vieira, A.J. Lichtenberg, R. Sherman, M. A. Lieberman, J. Y. Huang, W. Wonchoba, M. Steinberg and P. Khoury, to be given at the first international chaos conference, oct 1991.
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3.6 Experimental Realization Of Synchronization To A Chaotic Signal

The foundations for much the current work of our group on coupled phase lock loops has been G. Bernstein's thesis (ref 1), in which the chaotic behavior of a single digital phase lock loop fed with an external signal is described. The simple circuit described in the reference consists of an external input to a sample and hold circuit whose output, after being offset with an operational amplifier, feeds into a voltage controlled oscillator (VCO) which then retriggers the sample and hold circuit. The circuit itself has only one adjustable parameter; a potentiometer controlling the offset voltage provides a way of changing the behavior of this circuit. The only other factor which changes the circuit's behavior is the amplitude of the input waveform, which can be adjusted externally.

Because the proposed communications system uses two coupled phase lock loops as a central transmitting element, the proper functioning of this communications system depends on understanding the dynamics of the coupled loops. The dynamical equations contain four parameters. The values of these parameters will determine the behavior of the two loops. For some sets of values the two loops will be locked together each producing the same periodic output. When adjusted to a different set of values, the output of the two loops might seem chaotic. It is essential to know the behavior of the loops as a function of these four parameters so that a good operating point can be chosen; one where the signal can be efficiently incorporated and yet remain hidden.

Each of the four mathematical parameters in the equations should correspond physically to a way of adjusting the circuit. Simply putting two of the circuits described in reference 1 together leaves only two ways of tuning the circuit; the offset voltages of either loop can be adjusted independently of one another. The second two parameters correspond to the external adjustment of input amplitude in the circuit described by Bernstein. This additional degree of control, which had been external to the single PLL circuit before, now had to be incorporated in to the coupled loops. Adding two new potentiometers gave complete control over the circuit. (See figure 1) This new degree of freedom allowed tentative confirmation of computer simulations described in reference 3. (see figures 2 & 3) Distinct similarities can be observed between simulation and experiment. Both graphs exhibit a shift in phase from 0.25 to 0.75 which occurs at B of 0.2. Both also undergo a bifurcation near B of 0.5.

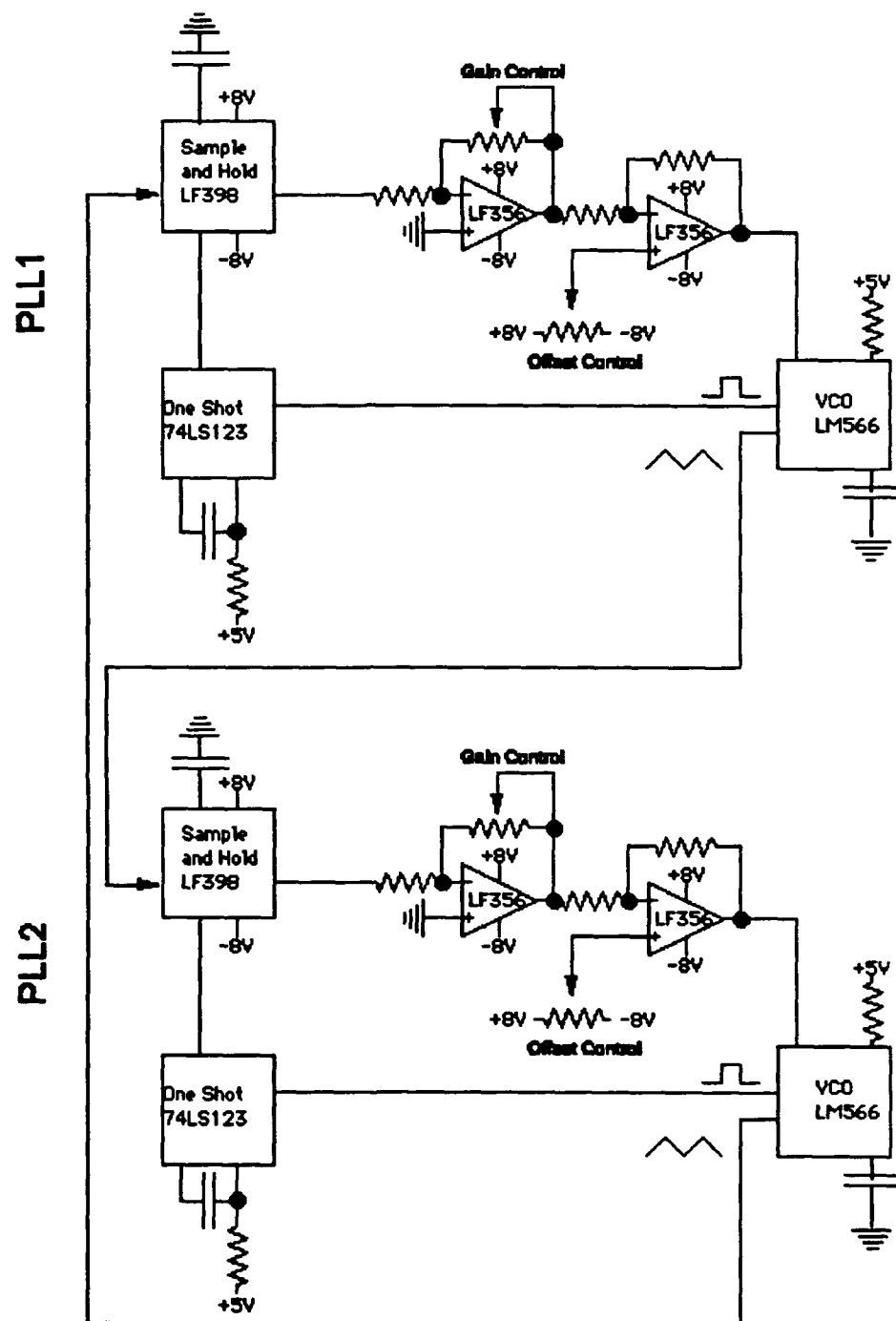


FIGURE 60. Coupled PLLs With Four Adjustable Parameters

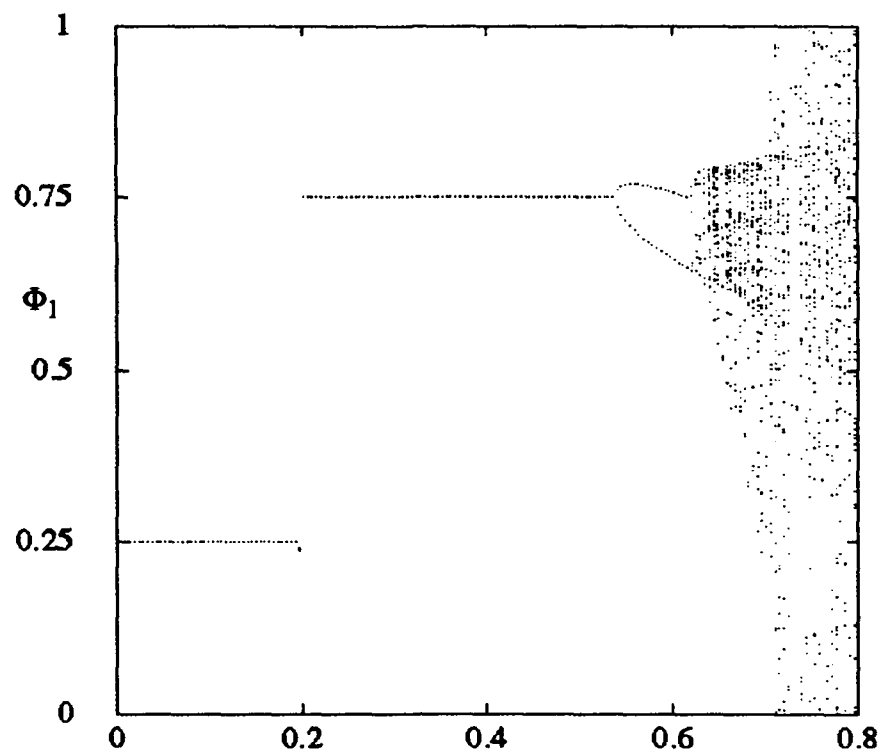


FIGURE 61. Theoretical Bifurcation Diagram For Coupled DPLLs

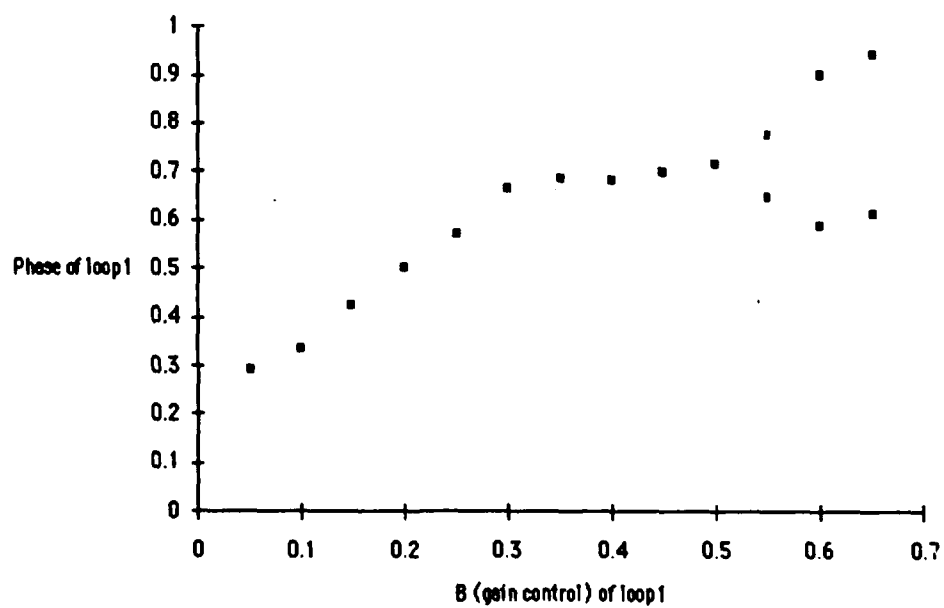


FIGURE 62. Experimental Bifurcation Diagram For Coupled DPLLs (Manual)

REFERENCE 1. G. Bernstein, Nonlinear Oscillation, Synchronization and Chaos; Thesis University of California, Berkeley (1988)



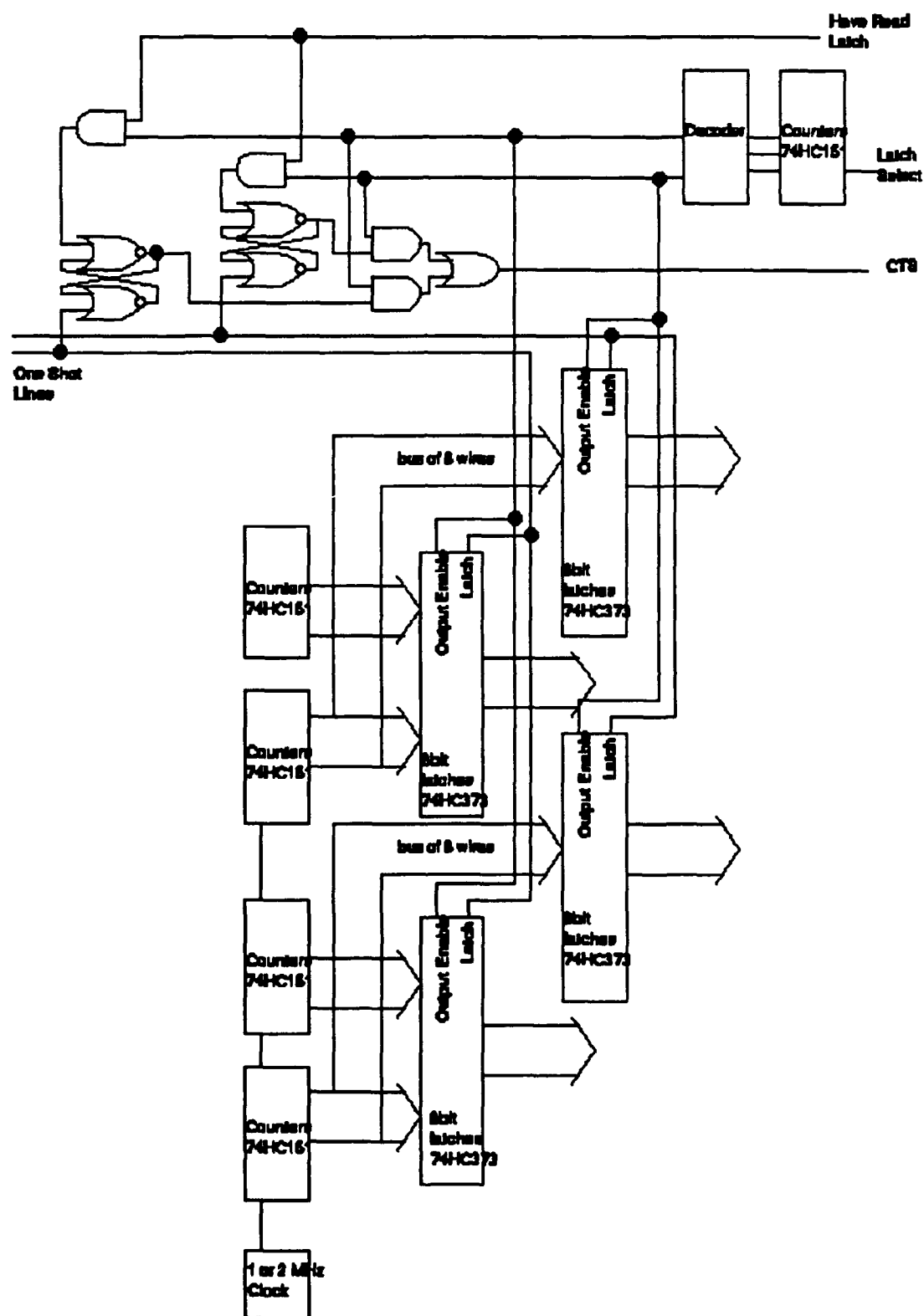


FIGURE 64. Digital Circuitry For Control Of DPLLs

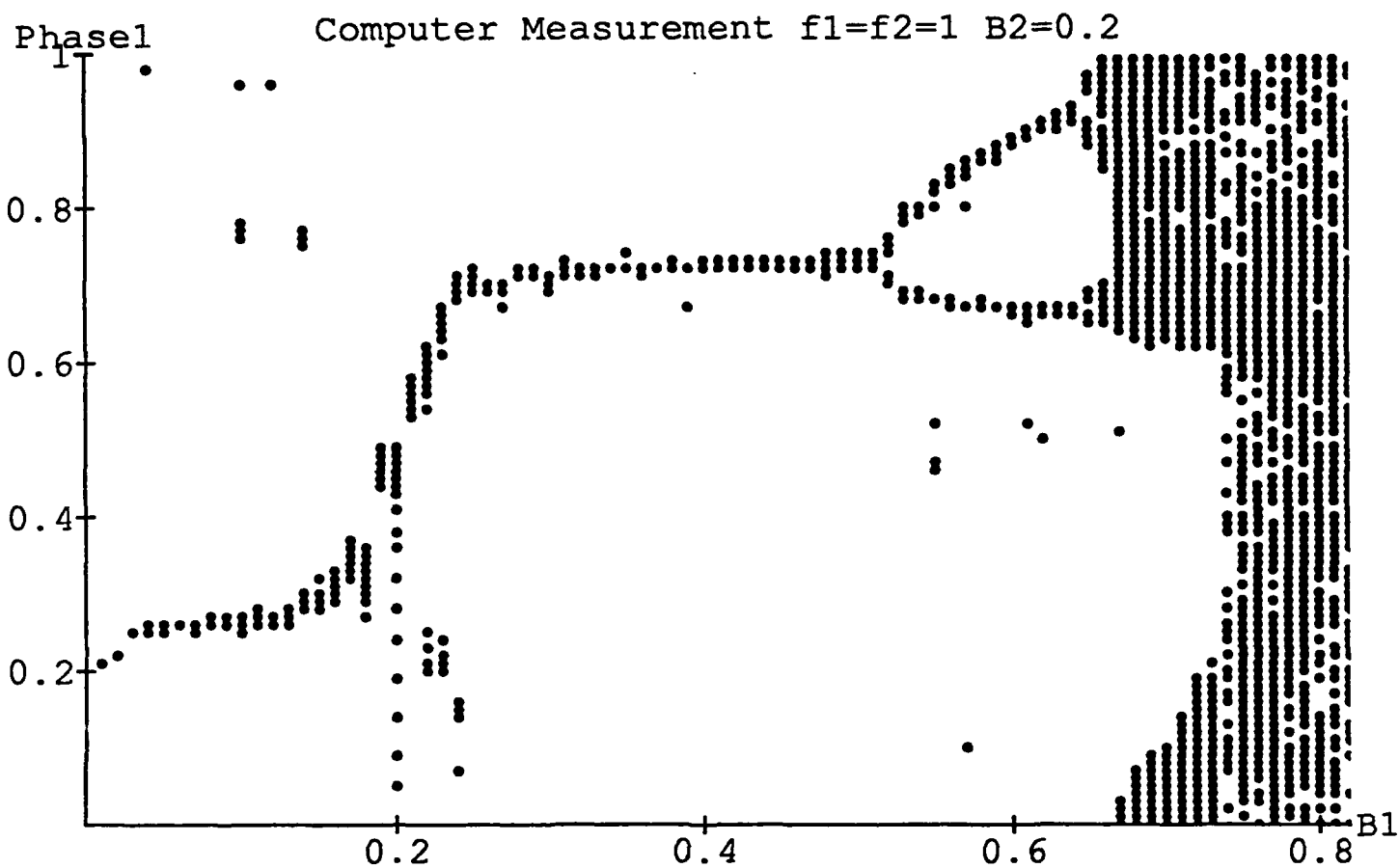


FIGURE 65. Computer Controlled Measured Bifurcation Diagram For Coupled DPLLs

3.7 A Novel Method For The Generation Of Pseudo Noise Sequences

3.7.1 INTRODUCTION

In spread spectrum systems, the pseudo-noise (PN) codes needed for signal spectrum spreading are, in general, generated from n -stage shift registers with either linear or non-linear feedback. FIGURE 66. below shows such a device. It is a finite state machine consisting of n consecutive 2-state memory units regulated by a single clock. At each clock pulse, the state(1 or 0) of each memory stage is shifted to the next stage in line, and the value of the Boolean function $f(\{x\})$ becomes the new state for the first stage while the content of the last stage is outputted to generate the PN sequence

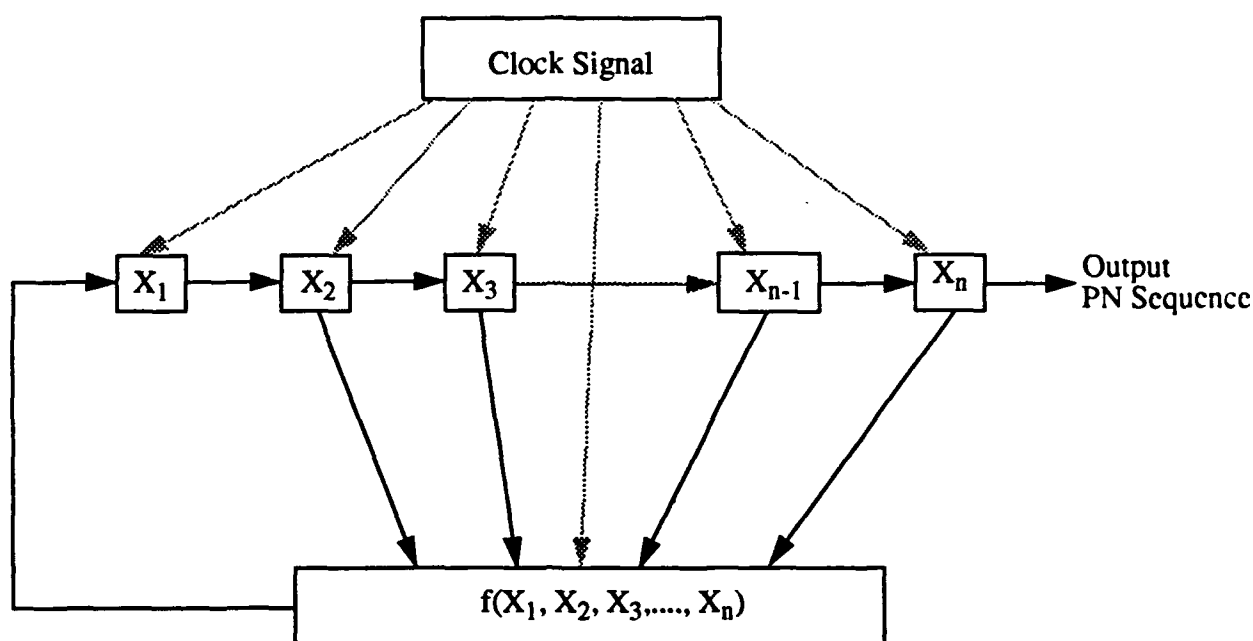


FIGURE 66. Feedback Shift Register For Generation of Pseudo-Noise Sequence.

It is obvious that the sequence generated by the n -stage shift register with feedback is periodic whose period can not be longer than 2^n . It is well known that sequences of length $2^n - 1$ can always be obtained from an n -stage register by mean of a feedback logic consisting entirely of modulo-2 additions (or linear logics, as they are also called). The number of linear logic functions yielding the maximum length of $2^n - 1$ is known to be exactly $r(2^n - 1)/n$, where r is Euler's function and is approximately equal to 2^n for large n . When the restriction of the feedback logic being linear is removed, the number of maximal-length shift register codes of degree n is increased to exactly $2^{2^n - 1} / 2$. This astronomical increase in the number of good codes leads many researchers to search for practical nonlinear shift registers. It is well to point out, however, that the period of these sequences is still limited to $2^n - 1$, where n is the stages of the register. (See [1].)

In this section we present a circuit consisting of N first order digital phase-locked loops (DPLL's) connected in a ring configuration with one of the PLL's having a positive Lyapunov exponent as shown in FIGURE 67. below. Where each of the digital phase lock loop consists of a phase detector, and a voltage-controlled oscillator or an A/D converter

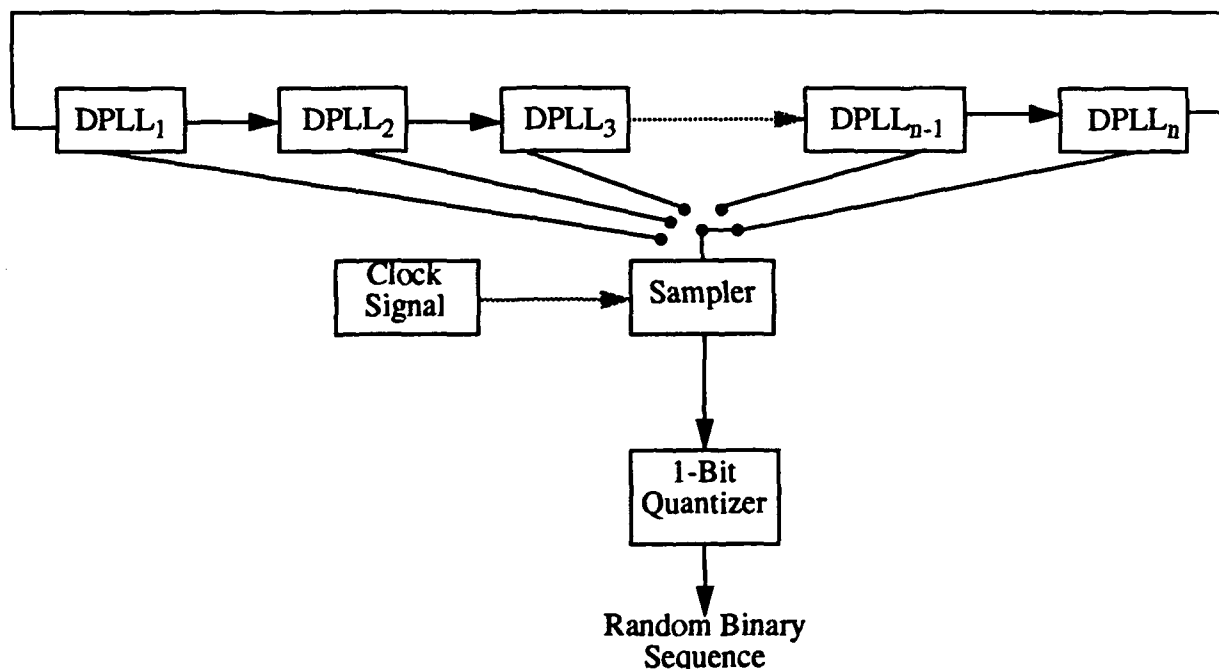


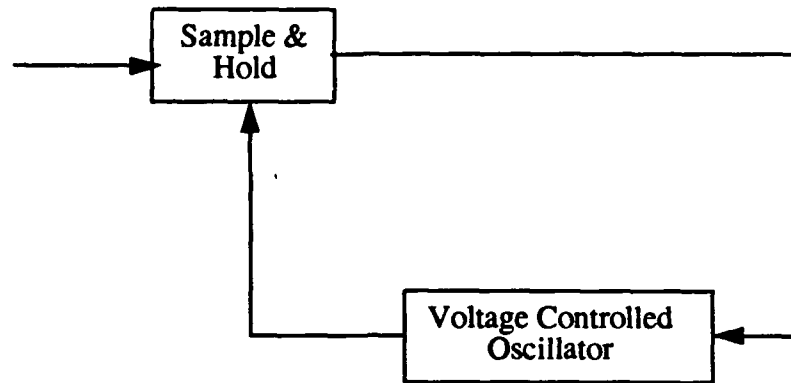
FIGURE 67. A Pseudo-Noise Sequence Generator Employing N Digital Phase Locked Loops (DPLLs) Connected in Ring Configuration With the n -th DPLL Having Positive Lyapunov Exponent

and a number-controlled oscillator (NCO) as shown in FIGURE 68. The output of any one of the DPLLs in the circuit is then be sampled at a rate equal to a small fraction, say 0.1, of the nominal frequency of the DPLLs, and each of the samples are quantized into a binary digit of 1 or 0, depending on the sample being positive or negative, respectively. The binary sequence so generated has the potential of being truly random with a long period. In the sections to follow, the operations of the circuit is described in detail and an algorithm is presented by which two identical circuits can be brought into synchronization, both for the clock signals and code phases. Also presented are the simulation results giving the properties of these sequences, including statistics on 0/1 balance, run lengths, auto-correlation and cross-correlation histograms.

3.7.2 A Novel Method for Generation of PN Sequences

In FIGURE 67. each of the digital phase-locked loops (DPLL's) is a digital processor performing the same functions as that of a first order analog phase locked loop. The loop consists of a sampler, an A/D converter, and a number controlled oscillator (NCO) as shown inFIGURE 68.(b). The nominal frequency of the NCO is $2\pi f_0$ radians per second when the external control voltage is zero, and its output is a sinusoid. The instantaneous frequency of the NCO is up-dated whenever its output has zero value with positive slope.

(a). Using Voltage-Controlled Oscillator.



(b). Using Number Controlled Oscillator.

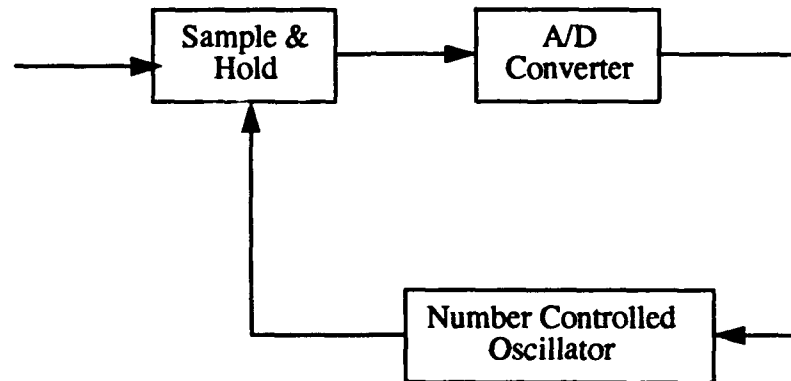


FIGURE 68. First Order Digital Phase Lock Loop

The new frequency of the i -th loop is given by

$$\omega(i,j) = 2\pi f_o + b(i,i-1) \times \sin[\omega(i-1,j) \times t(i,j) + \phi(i-1)]$$

for $i = 2, 3, \dots$, and

$$\omega(1,j) = 2\pi f_o + b(1,n) \times \sin[\omega(n,j) \times t(1,j) + \phi(n)]$$

Where:

$b(i,j)$ = coupling coefficient between the i -th and j -th loops,

$\omega(i,j)$ = the angular frequency of the i -th loop at the j -th sampling instant,

f_o = the nominal frequency of the NCO's, in Hz,

$t(i,j)$ = the j -th sampling time for the i -th loop,

and

$\phi(i)$ = the initial phase angle of the i -th loop output.

The sampler of the i -th DPLL would sample the input voltage from the $(i - 1)$ st DPLL at the above-described time instant, the sampled voltage is quantized into M -bit word, and the M -bit binary word is fed to the input of the NCO to cause a change of its frequency. Therefore, the frequency of each NCO changes every time it has produced one cycle of sinusoidal signal.

The clock signal, whose period is nearly one order of magnitude shorter than the nominal periods of the DPLLs (i.e. $1/f_0$), is used to clock the output of any one of the DPLL's to the 1-bit quantizer, and produce, at the quantizer's output, a binary sequence.

Note that the system of FIGURE 67. is similar in structure to the system of shift registers with feedback depicted in FIGURE 66. Both systems are finite state autonomous machines with the code period of the binary sequence generated by the feedback shift register being limited by the stages in the system. However, by replacing the two-state memory units by DPLLs and properly choosing the coupling coefficients (the b s), it is possible to have the second system behave as a chaotic system. As a consequence, the binary sequences so generated could be completely random, with periods of nearly infinite duration. Further the period would be independent of the number of DPLL's in the system, provided that the system contains at least two DPLL's and one of the DPLL is operated in a chaotic mode (i.e. having a positive Lyapunov exponent). If the sequences so generated are to be truly random, they must have the following properties:

- 1). The number of 1's and 0's in a sequence be nearly the same, i.e the probability of 1's and the probability of 0's in the sequence each be nearly equal to 0.5.
- 2). Runs of consecutive 1's or of consecutive 0's frequently occur, with short runs being more frequent than long runs. More precisely, about one-half the runs should have length 1, one-fourth should have length 2, one-eighth should have length 3, etc.
- 3). The auto-correlation functions of the sequences should have value of 1 when code phase shift is zero and nearly 0 when the shift is non-zero. That is to say: If we let $\{a_m\} = \{a_1, a_2, a_3, \dots\}$ be a binary sequence, and the auto-correlation function of the sequence, $A(k)$, is defined as

$$A(k) = \lim_{M \rightarrow \infty} \frac{1}{M} \sum_{m=1}^M a_m a_{m+k}$$

Then the desired property of the sequence is that the value of $A(k)$ be 1 for $k = 0$ and very small for all other values of k .

4). The cross-correlation function of two different sequences should be nearly equal to zero for all code phase shifts. If we let $\{a_m\} = \{a_1, a_2, a_3, \dots\}$ and $\{b_m\} = \{b_1, b_2, b_3, \dots\}$ be two different binary sequences, and the cross-correlation function of the two sequences is defined as

$$C(k) = \lim_{M \rightarrow \infty} \frac{1}{M} \sum_{m=1}^M a_m b_{m+k}$$

Then $C(k)$ measures the amount of similarity between the two sequences, for all values of code phase shifts. $C(k)$ should be very small for all integer values of k , including k equal to zero.

It shall be shown later that the sequences generated by the DPLL's connected in the ring configuration have all the properties given above.

3.7.3 An Algorithm for Synchronization of Two Identical Chaotic Systems.

The chaotic system described in section 3.7.2 for generating PN sequences for use in a spread spectrum communication system is useful only if the PN code can be reproduced exactly. This includes perfect code phase synchronization by another (identical) system used as a PN code generator, at a receiver, for the purpose of PN code despreading. Given below is a method by which two identical chaotic systems can be made to synchronize to each other.

The two systems are initially set to have identical initial conditions, i.e. the corresponding DPLLs in both systems are to have the same initial frequencies and phase angles. Let the first system to be the one generating the transmitting PN code, and the second system is to generate a binary code sequence in synchronization with the transmitted code. Initially, the first system is to repeatedly generate a code sequence of N_w code chips by resetting the system to its original initial conditions right after generating N_w code chips. In the meantime, the second system also generates N_w code chips. It performs cross-correlation of the received code sequence and its own generated code chips, using N_w parallel digital processors for each of the N_w different code phases. It seeks the particular code phase that gives the maximum correlation value. The peak correlation value will be initially quite small because two clock signals are likely to be out of synchronization. Next, the receiver's clock signal is advanced by 'x' percent of the clock period, and another sequence of N_w code chips is generated, cross-correlation of the two sequences is again performed, and the code phase with the largest correlation value is identified. The two correlation peaks are compared and the one with the largest value with its corresponding code phase position is retained. This process is repeated until the phase of the receiving clock signal is advanced by one period. By this time, the code phase synchronization would have been achieved with the two clock signals being out of phase by no more than one half of 'x' percent of the period of the clock signal, provided that the clock signal phase error is sufficiently small. A second pass of the clock phase search may be required. This could be done by advancing the receiving clock signal phase by one-tenth of the original time increment around the correlation peak time instant obtained in the first pass. This process is

continued until the correlation peak exceeds a certain threshold value, at which time both clock signal phase and code phase synchronizations would have been achieved. Soon after the correlation peak exceeds the threshold setting, the transmitter is signalled by the receiver to this effect and both PN code generating systems are turned into normal operating mode. At the same time the receiver is switched from the acquisition mode to a tracking mode and normal data transmission can be initiated.

It takes $N_w T_c$ seconds to perform correlation of N_w chips, where T_c is the code chip time interval. Hence, it takes $100N_w T_c/x$ seconds to complete the first pass of the clock phase search over one clock period. In the second and subsequent passes, however, it should take no longer than $20N_w T_c$ second to complete a pass. This is because the clock phase search time interval has been narrowed down to within twice the previous search time increment. This assumes that the increment is reduced by a factor of 10 in each of the successive passes.

It is well to point out that in order to minimize the probability of false synchronization and to maximize the probability of correct synchronization, a more elaborated scheme such as multiple sequential detection method must be used. See reference [2] for additional information.

In the simulations of the acquisition and synchronization of the transmitting and receiving PN codes, to be detailed in the next section, it has been found that no more than three (3) passes were required to achieve synchronization. Synchronization was considered to have occurred when the correlation peak was greater than 0.99. During these simulations the input signal-to-noise ratio (SNR) was -10 dB or higher. The correlation window, N_w , was equal to (or longer than) 512 code chip, and the initial clock signal phase search increment, ΔT_s , was no greater than one (1) percent of the clock signal's period, i.e., $\Delta T_s < .01T_c$.

3.7.4 Simulation Results.

In order to investigate the properties of random sequences generated by the system of FIGURE 67., simulations were performed for systems with two (2) or four (4) DPLLs. Sequences of lengths nearly equal to 250,000 code chips, for various coupling coefficients, were generated. In all cases, the DPLL with the highest index was the one having positive Lyapunov exponent i.e. was operating in a chaotic mode. All the other DPLLs had negative Lyapunov exponents and were thus operating in stable regions. The nominal frequencies of the NCO's were all taken to be one (1) radian/second, and, consequently, the clock signal period were in the range of 40 to 100 seconds.

The next few subsections contain details of the simulation results. This includes; correlation peaks versus the clock phase (timing) error, synchronizations of code and clock phases, statistics of 0/1 balance, run length, and auto-correlation and cross-correlation of various code sequences generated from the output of the DPLL with positive Lyapunov exponent. The simulations were performed using the following set of system parameters.

2-DPLL System:

Code No. 1: $b_1 = .32$, $b_2 = .65$, and clock period = 70 seconds

Code No. 2: $b_1 = .37$, $b_2 = .63$, and clock period = 70 seconds

4-DPLL system:

Code No. 3: $b_1 = .32$, $b_2 = .28$, $b_3 = .24$, $b_4 = .67$, and clock period = 70 seconds

Code No. 4: $b_1 = .31$, $b_2 = .28$, $b_3 = .24$, $b_4 = .67$, and clock period = 45 seconds

Code No. 5: $b_1 = .32$, $b_2 = .25$, $b_3 = .20$, $b_4 = .67$, and clock period = 45 seconds

Code No. 6: $b_1 = .32$, $b_2 = .25$, $b_3 = .20$, $b_4 = .67$, and clock period = 70 seconds

These parameter sets were chosen for the purpose of determining whether the generated codes have good auto-correlation and cross-correlation properties. Because of this some of the parameter sets are very nearly the same.

Correlation Peaks versus Clock Phase (Timing) Error

FIGURE 69. through FIGURE 80. show graphs of the positive and negative correlation peaks versus the normalized clock timing error. The number of code chips being correlated, i.e., the correlation window, was either 512 or 1024 chips and there were various values of clock's signal period. In all cases shown, the input signal-to-noise ratio (SNR) is 50 dB or higher and, therefore, can be considered to be noiseless. It is seen that the positive correlation peak of unity always occurs when both code and clock signal phases are in perfect synchronization. However, when the clock phase (timing) error is non-zero, the correlation peak can occur at places where the code phase errors may be non-zero.

FIGURE 69. and FIGURE 71. show the positive and negative correlation peaks vs. clock phase error for the 2-DPLL system where the binary code sequence is generated from the output of the DPLL with positive Lyapunov exponent (the second DPLL). FIGURE 70. and FIGURE 72. are for the cases where the code sequence is generated from the output of the DPLL with negative exponent (the first DPLL). It is seen that the code sequence generated from the second DPLL gives only one positive correlation peak at zero clock phase error and two negative correlation peaks at clock signal phase error of about one-tenth of the clock period. For the code sequence generated from the first DPLL, however, it is seen that there is a positive correlation peak of unity at the zero clock phase error in addition to many other local peaks at places where clock phase error is non-zero. This sequence gives two dominant negative peaks at two values of clock phase errors whose absolute values are equal to one-twentieth of the clock period, and many other side lobes. This peculiar phenomenon is also observed for the 4-DPLL system. (See FIGURE 73. to FIGURE 80.). From these observations we can conclude that the code sequences generated from the output of the chaotic DPLL has better correlation properties thus preventing the system from

falsely locking into the local positive peak during the acquisition phase, and consequently requiring a shorter acquisition time.)

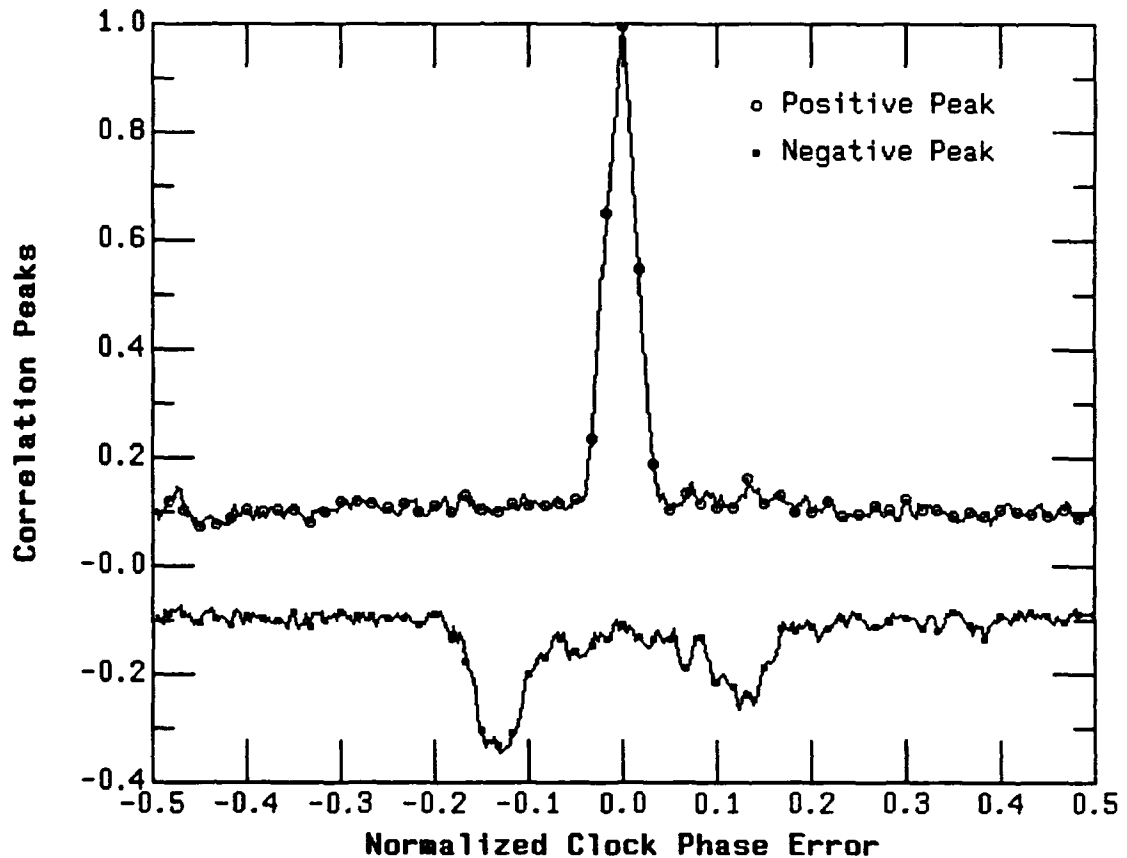


FIGURE 69. The Correlation Peaks Versus the Clock Phase Error of the Code Sequence Generated From the Output of the Second DPLL of the 2-DPLL System $b_1 = .32$, $b_2 = 0.65$, and Clock Period= 60 seconds. [Correlation window = 512 code chips.

FIGURE 81. through FIGURE 84. show the expanded version of FIGURE 69., FIGURE 71., FIGURE 73., and FIGURE 75., respectively, near the zero clock phase error. It is seen that in order to have the positive correlation peak remaining greater than 0.8, the clock phase error must be kept to within one (1) percent of the clock period. Hence, in the process of establishing code and clock signal phase synchronizations with input thermal noise, the clock timing should be advanced by an increment no larger than 0.01 times the clock period so that the desired synchronizations can be achieved within a few passes using the algorithm described in section 3.7.3

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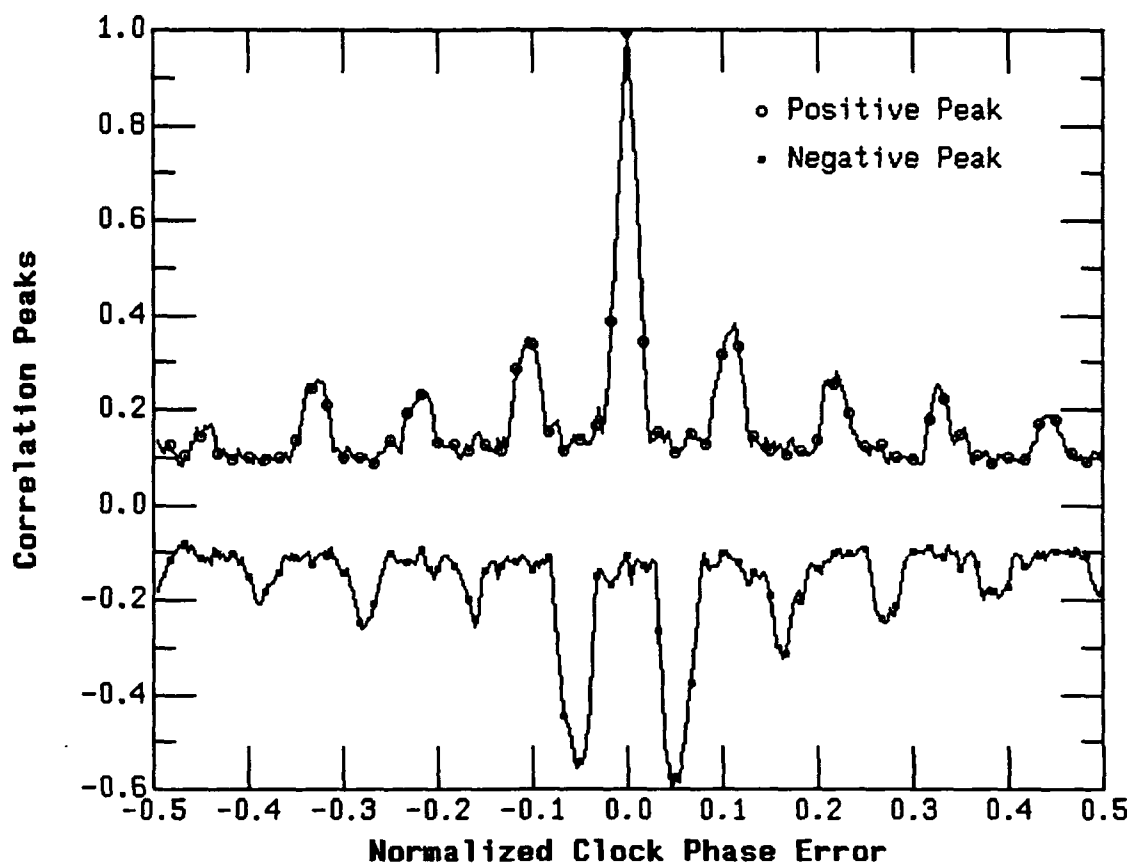


FIGURE 70. The Correlation Peaks Versus the Clock Phase Error of the Code Sequence Generated From the Output of the First DPLL of the 2-DPLL System With $b_1=.32$, $b_2=.65$, and Clock Period = 60 Seconds. {Correlation window = 512 code chips.

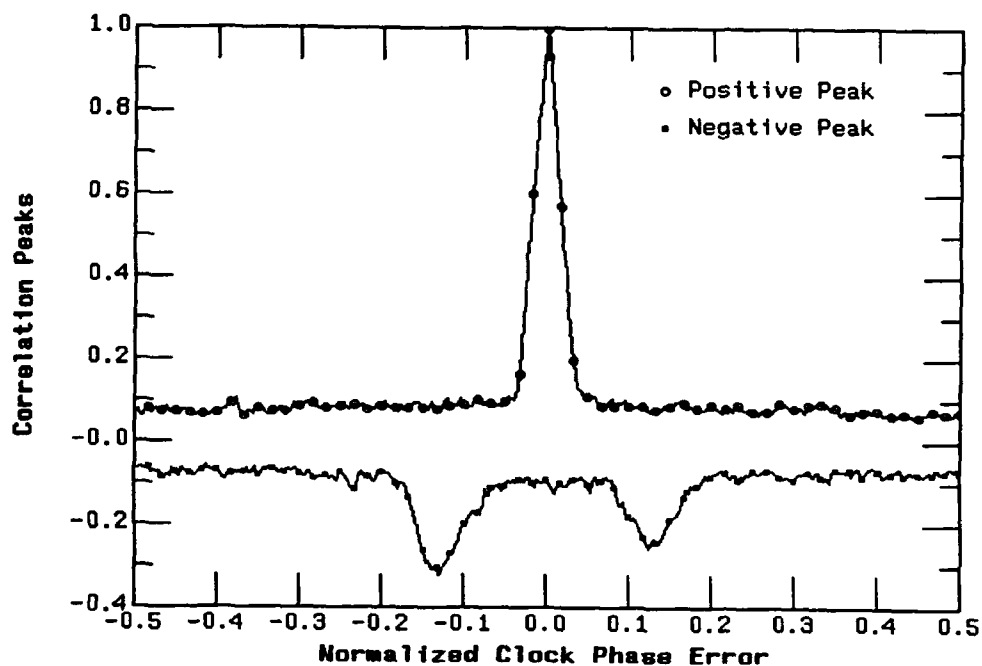


FIGURE 71. The Correlation peaks Versus the Clock Phase Error of the Same Code Sequence of FIGURE 69.[Correlation window = 1,024 code chips.

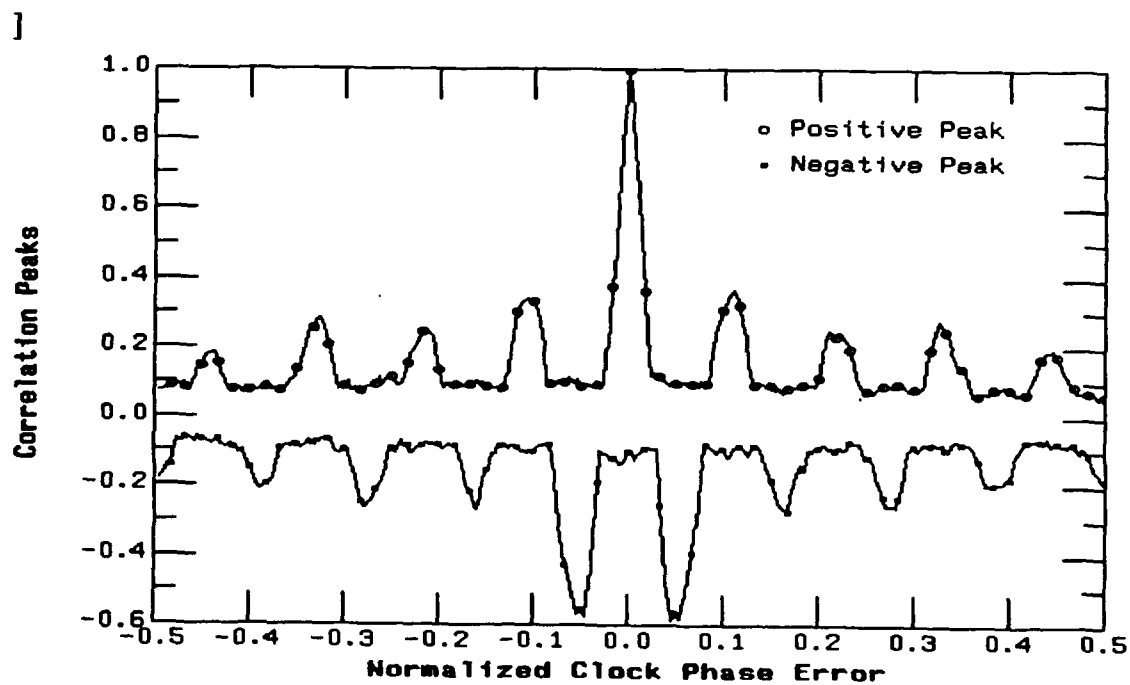


FIGURE 72. The Correlation Peaks Versus the Clock phase Error of the Same Code Sequence of FIGURE 70.[Correlation Window = 1,024 code chips

J

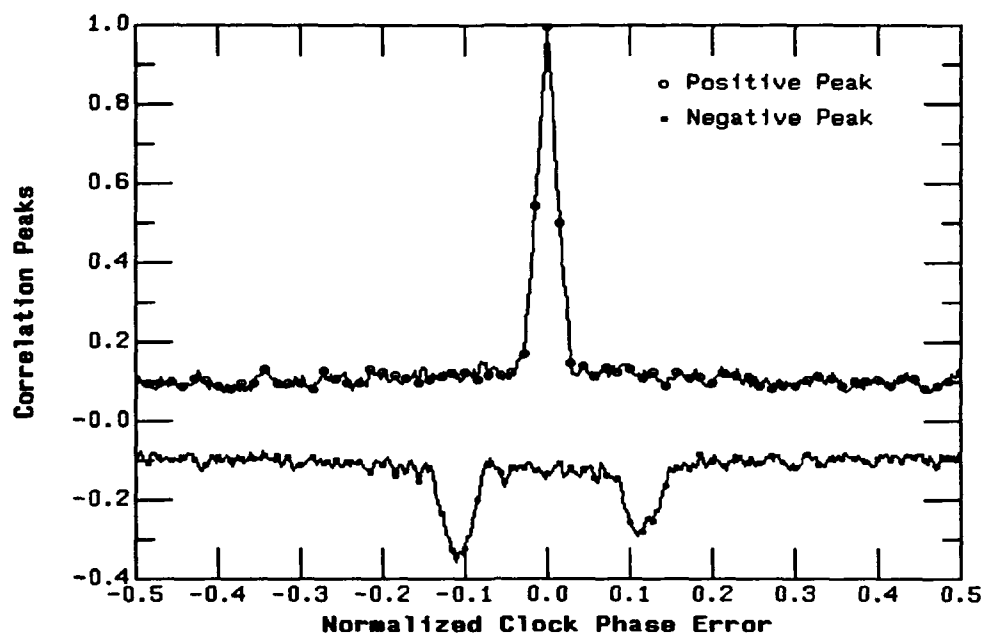


FIGURE 73. The Correlation Peaks Versus the Clock Phase Error of the Code Sequence Generated From the Output of the Fourth DPLL of the 4-DPLL system with $b_1 = .32$, $b_2 = .28$, $b_3 = .24$, $b_4 = .67$, and Clock Period = 70 seconds. [Correlation Window = 512 code chips.]

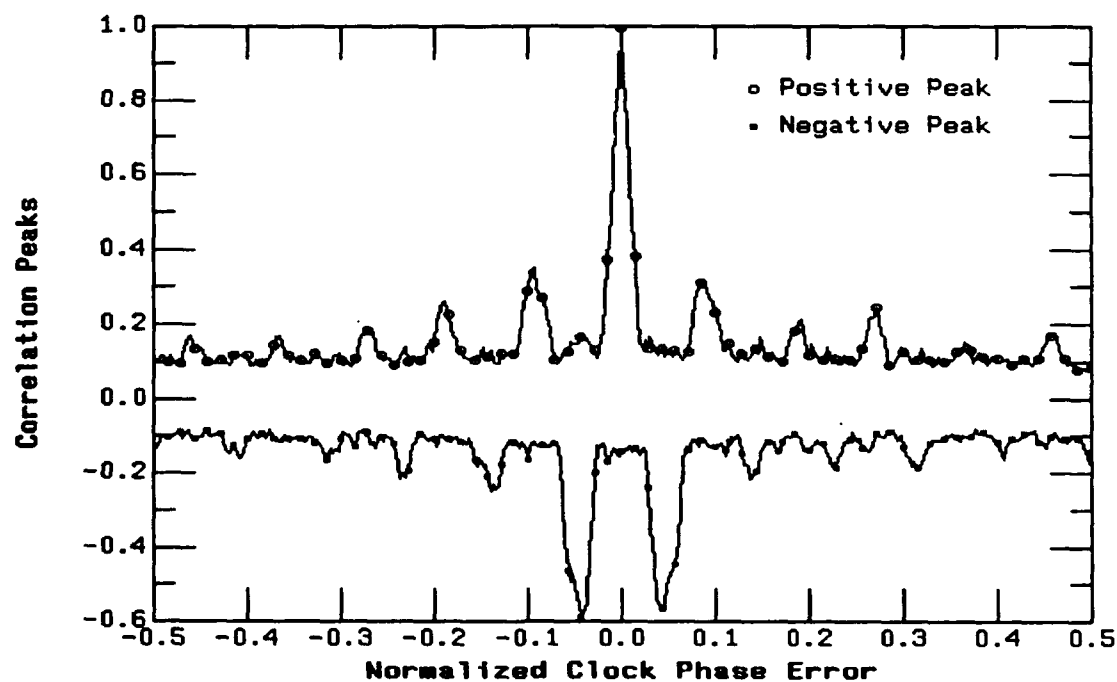


FIGURE 74. The Correlation peaks Versus the Clock Phase Error of the Code Sequence Generated From the Third DPLL of the 4-DPLL System with $b_1 = .32$, $b_2 = .28$, $b_3 = .24$, $b_4 = .67$, and Clock Period = 70 seconds. [Correlation window = 512 code chip]

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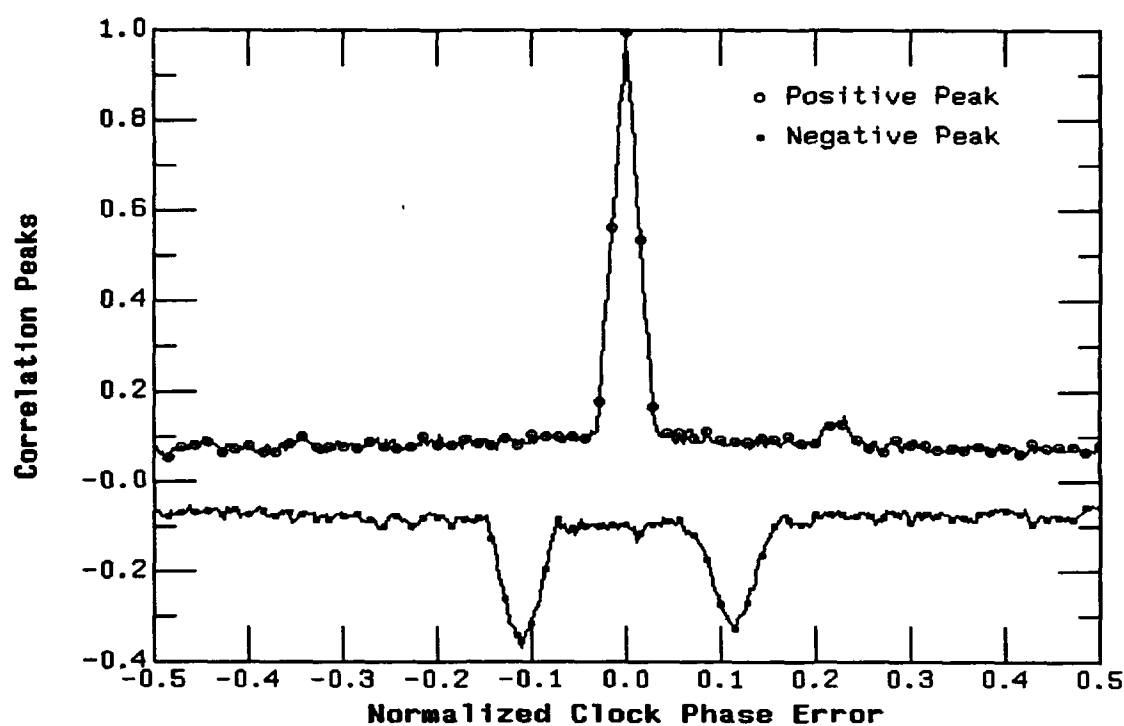


FIGURE 75. The Correlation Peaks Versus Clock Phase Error of the Same Code Sequence of FIGURE 73. [Correlation window = 1,024 code chips.

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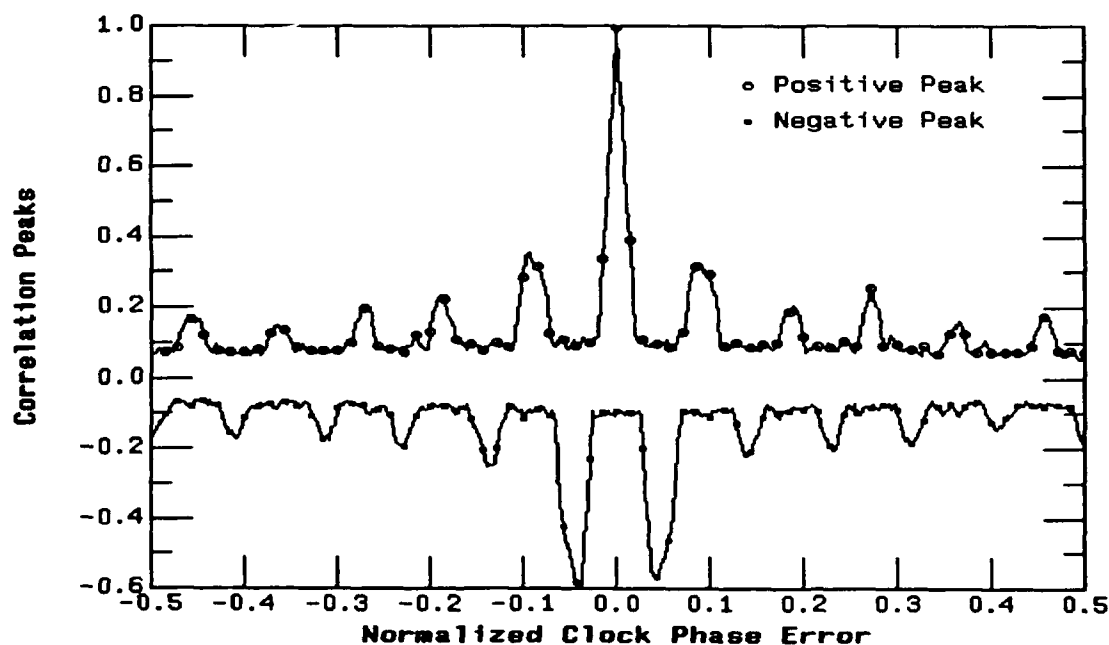


FIGURE 76. The Correlation Peaks Versus the Clock Phase Error of the Same Code Sequence of FIGURE 74. {Correlation window = 1,024 code chips.

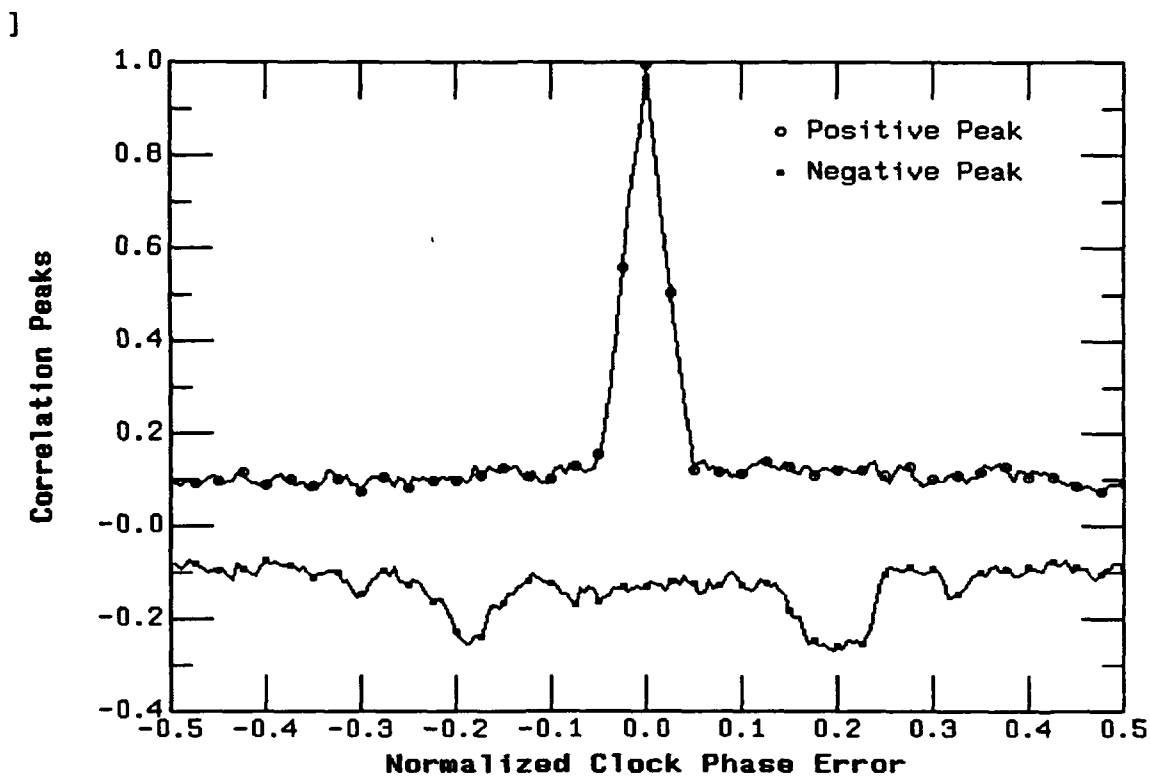


FIGURE 77. The Correlation Peaks Versus Clock Phase Error of the Same Code Sequence of Figure 4.1.5 Except the Clock Period= 45 Seconds. [Correlation Window = 512 code chips.

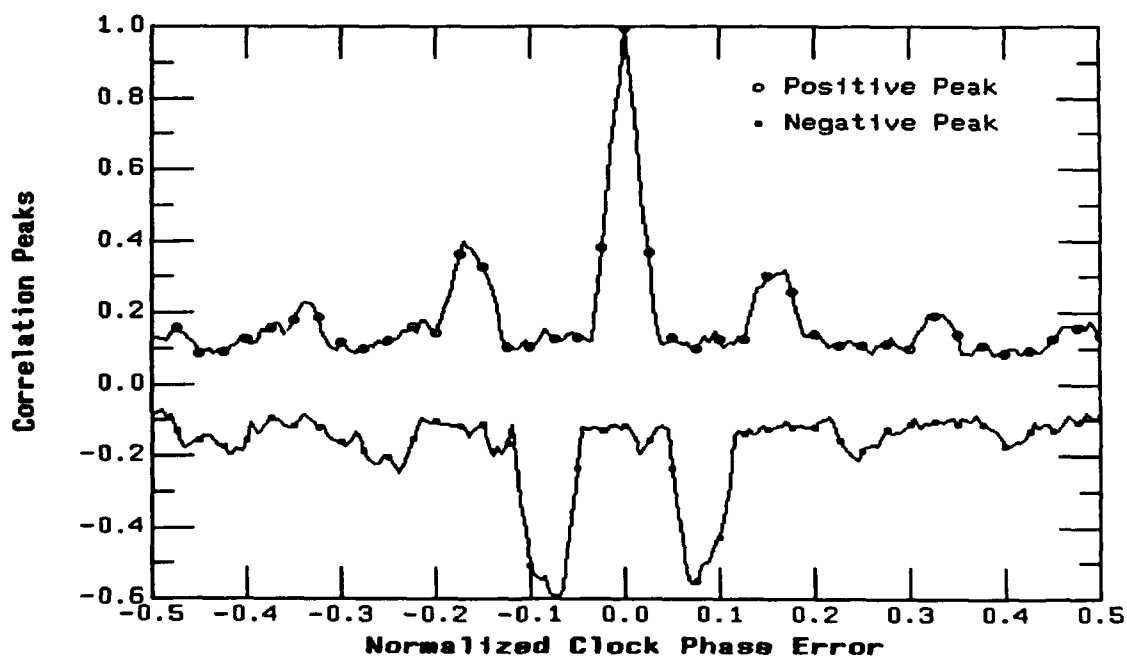


FIGURE 78. The Correlation Peaks Versus the Clock Phase Error of the Same Code Sequence of FIGURE 74. Except the Clock Period= 45 Seconds. [Correlation Window= 512 code chips

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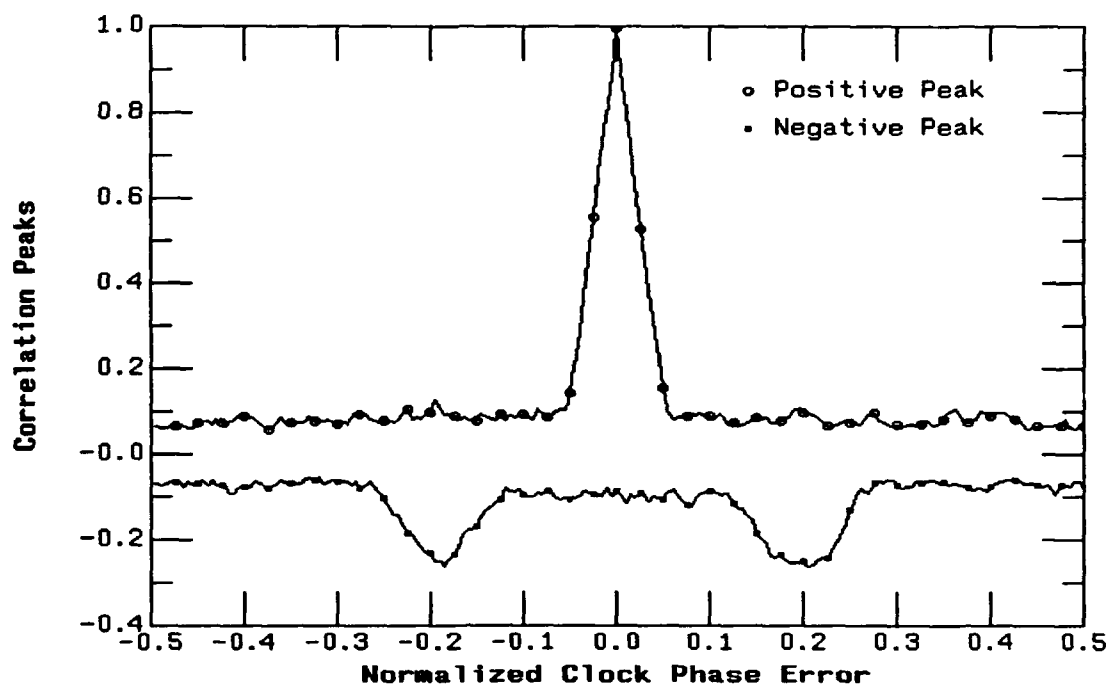


FIGURE 79. The Correlation peaks Versus the Clock Phase Error of the Same Code Sequence of FIGURE 77. [Correlation Window= 1,024 code chips.

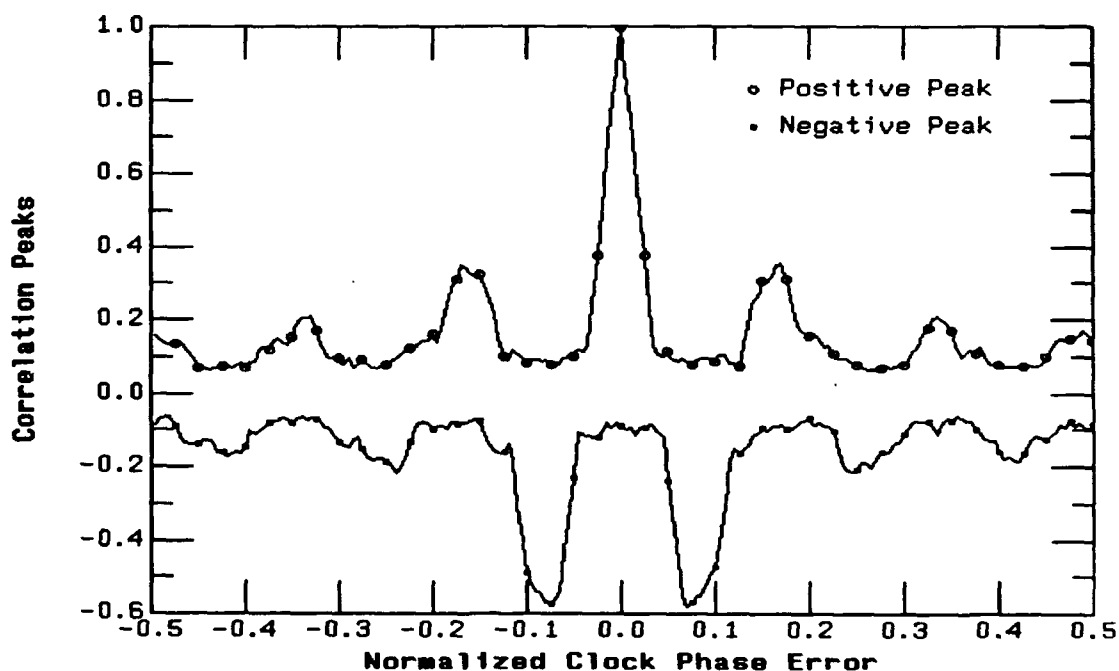


FIGURE 80. The Correlation Peaks Versus Clock Phase Error of the Code Sequence of Figure 4.1.10. [Correlation window= 1,024 code chips.

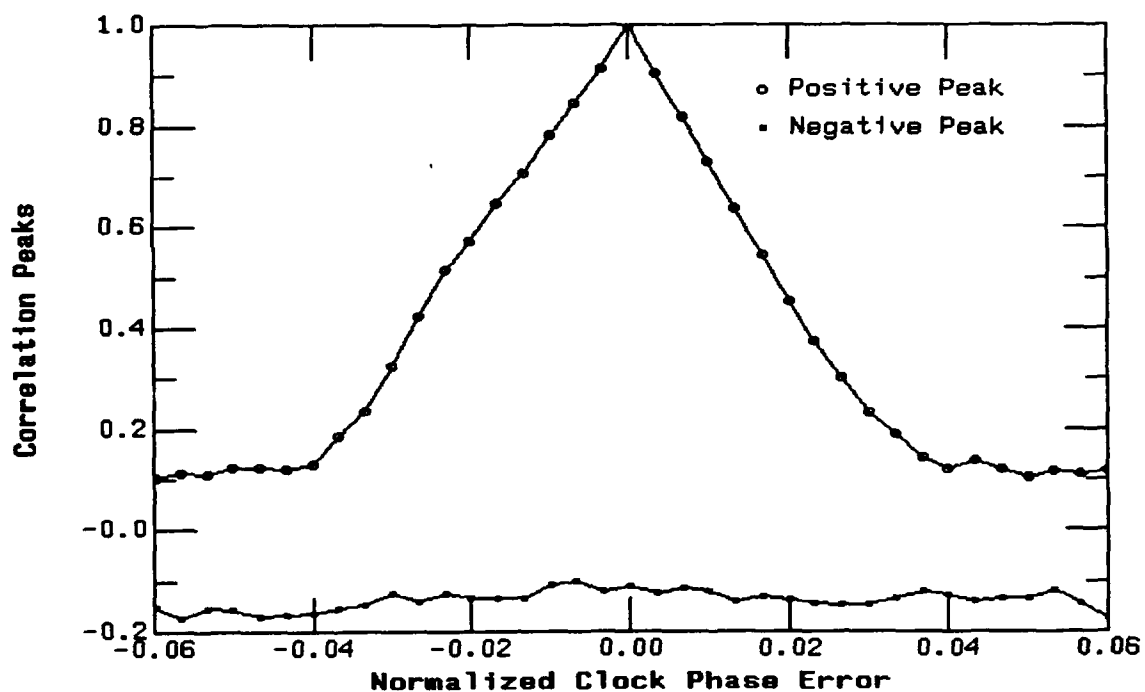


FIGURE 81. Expanded Version of FIGURE 69..

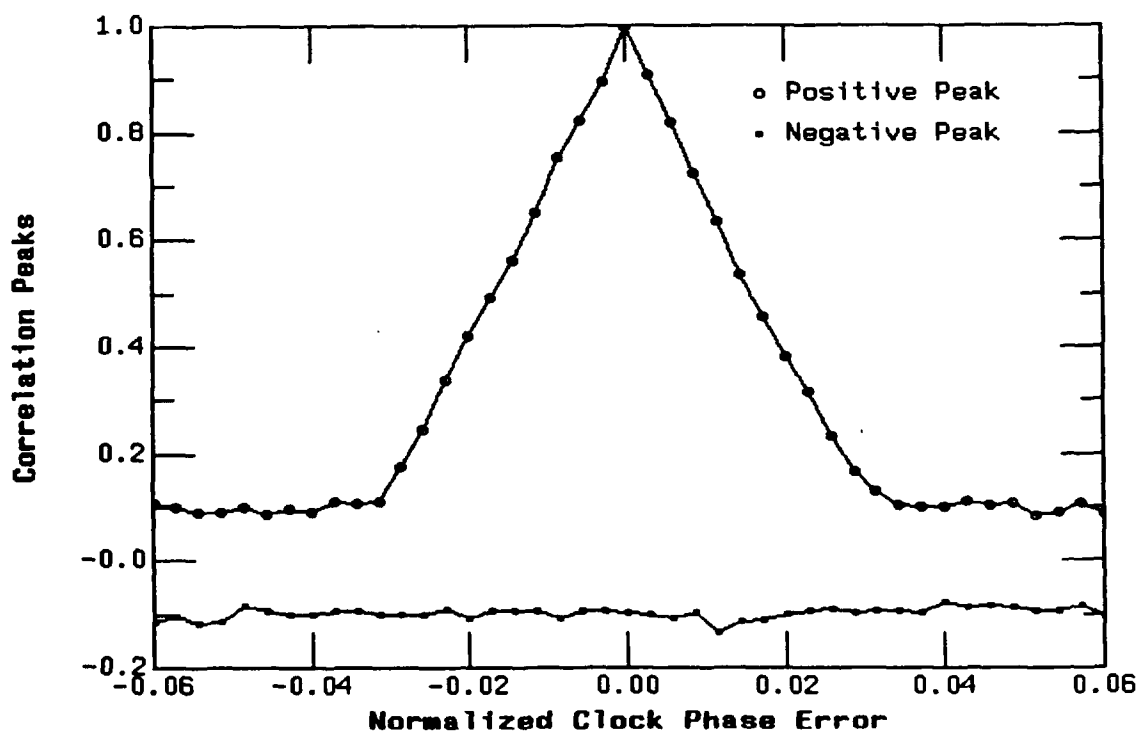


FIGURE 82. Expanded Version of FIGURE 71.

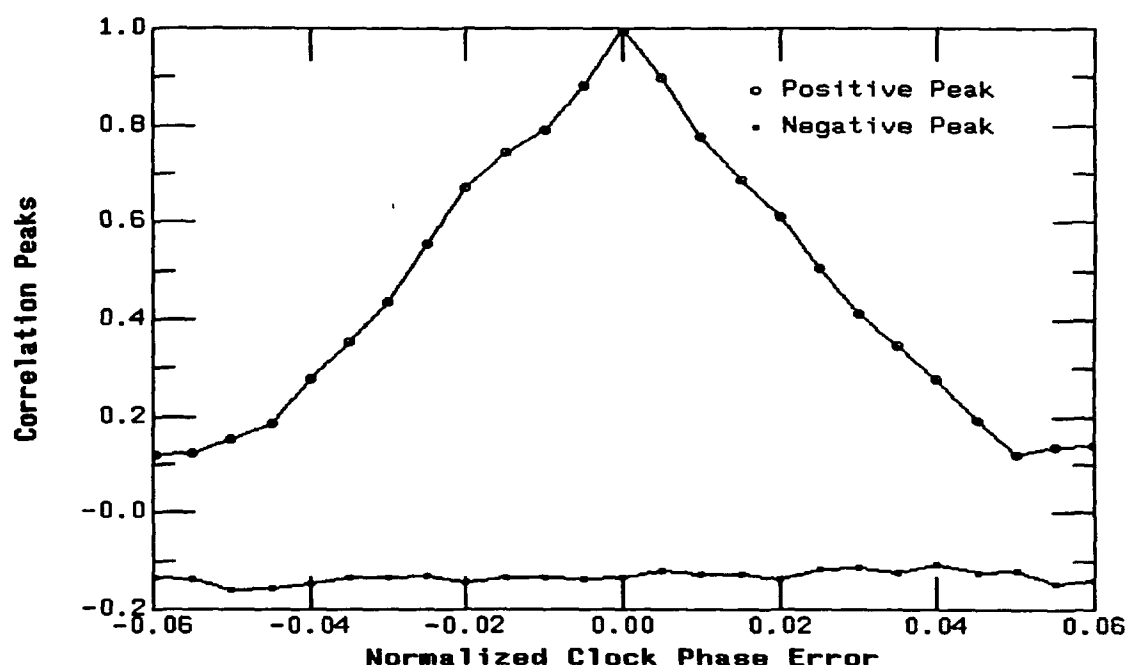


FIGURE 83. Expanded version of FIGURE 73.

3.7.5 Run Length And 0/1 Balance Properties Of Code Sequences

Given in this section are the run-length and 0/1 balance properties of the code sequences described in Section 3.7.4. All the sequences are generated from the 2-DPLL or 4-DPLL system with code length of $2^{18} = 262,144$ code chips. Each of the sequences have been checked to determine if the entire sequence contains subsequences of period 2^m for m between 9 and 17. No subsequences of such periods have been found and, therefore, it is reasonable to conclude that the sequences generated by these systems can have periods much longer than 2^{18} code chips.

Tables 1 and 2 give the 0/1 balance and run length properties of the Codes No.1 and No.2 sequences generated from the output of the DPLL with positive Lyapunov exponent of the 2-DPLL system. It is seen that these sequences have nearly balanced 1- and 0-bit, and their run lengths are very close to the ideal cases

.Tables 3 through 6 show the 0/1 balance and run length properties of Codes No.3 through No.6 sequences generated from the DPLL with positive Lyapunov exponent of the 4-DPLL system. Again, it is seen that the 0/1 balance of these sequences are nearly perfect. The run lengths for the sequences deviate from the ideal by no more than 10 percent for shorter run lengths of up to twelve (12) consecutive 0 or 1 code chips, and they differ from the ideal by as much as 100 percent for run lengths of sixteen and seventeen. It is well to point out, however, that probabilities of such long run lengths are of the order of ten to the negative 5 (10^{-5}).

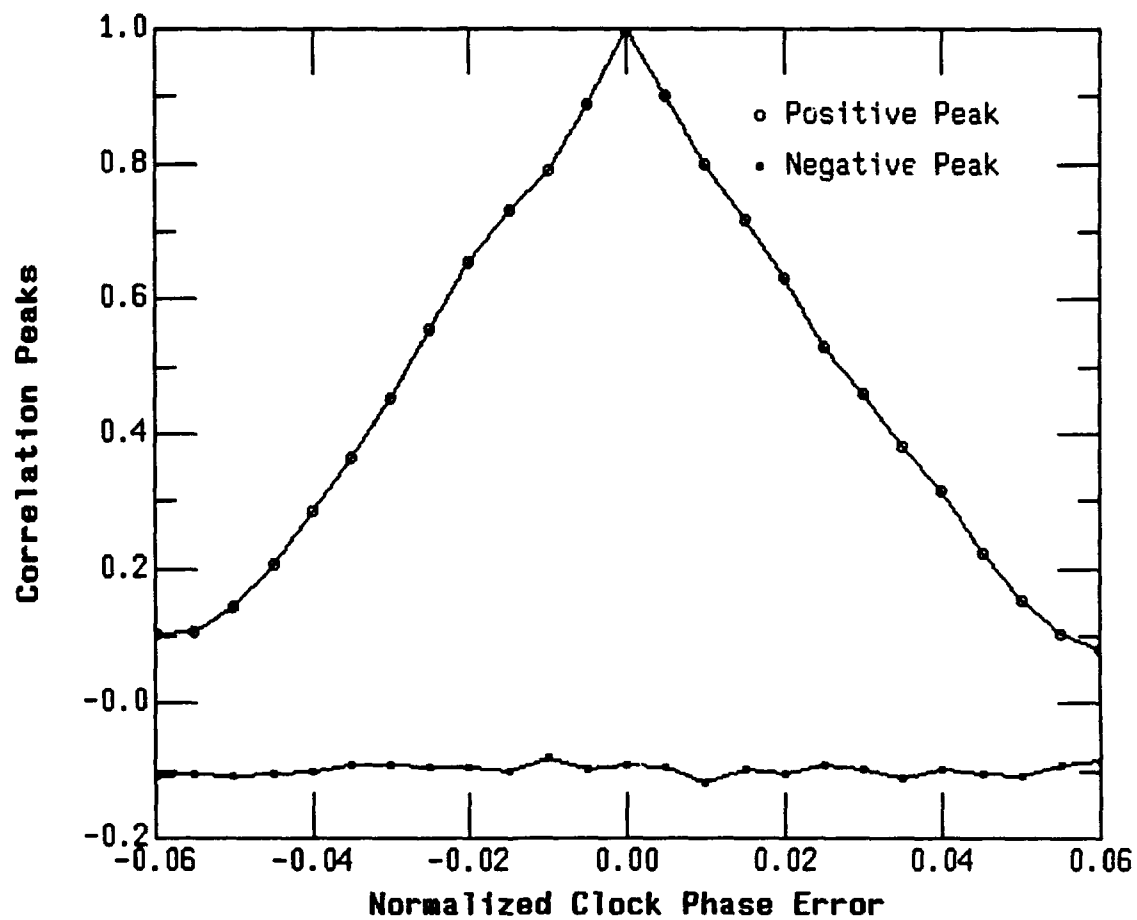


FIGURE 84. Expanded version of FIGURE 75.

Table 1. 0/1 Balance And Run Length Statistics of the Code No. 1.

1/0 Balance = 0.5003/0.4997

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2485659	0.2494773	0.4980432	0.5000000
2	0.1253398	0.1244438	0.2497836	0.2500000
3	0.0631371	0.0626852	0.1258223	0.1250000
4	0.0315839	0.0315992	0.0631830	0.0625000
5	0.0154013	0.0160447	0.0314460	0.0312500
6	0.0077428	0.0079572	0.0157000	0.0156250
7	0.0039824	0.0039365	0.0079189	0.0078125
8	0.0021674	0.0019682	0.0041356	0.0039062
9	0.0010952	0.0007965	0.0018917	0.0019531
10	0.0004748	0.0005361	0.0010109	0.0009766
11	0.0002527	0.0003063	0.0005591	0.0004883
12	0.0001379	0.0001379	0.0002757	0.0002441
13	0.0000460	0.0000613	0.0001072	0.0001221
14	0.0000306	0.0000077	0.0000383	0.0000610
15	0.0000077	0.0000153	0.0000460	0.0000153
17	0.0000077	0.0000000	0.0000077	0.0000076
18	0.0000000	0.0000000	0.0000000	0.0000038
19	0.0000077	0.0000000	0.0000077	0.0000019

Table 2. 0/1 Balance and Run Length Statistics of Code No. 2.

1/0 Balance = 0.5001/0.4999

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2584428	0.2577482	0.5161911	0.5000000
2	0.1283514	0.1288120	0.2571633	0.2500000
3	0.0591783	0.0593246	0.1185029	0.1250000
4	0.0279514	0.0286241	0.0565755	0.0625000
5	0.0136430	0.0133579	0.0270009	0.0312500
6	0.0064633	0.0065071	0.0129704	0.0156250
7	0.0032609	0.0029319	0.0061927	0.0078125
8	0.0014330	0.0014038	0.0028368	0.0039063
9	0.0006434	0.0007458	0.0013892	0.0019531
10	0.0003217	0.0002925	0.0006142	0.0009766
11	0.0001828	0.0001024	0.0002851	0.0004883
12	0.0000512	0.0000804	0.0001316	0.0002441
13	0.0000439	0.0000366	0.0000804	0.0001221
14	0.0000000	0.0000146	0.0000146	0.0000610
15	0.0000146	0.0000000	0.0000146	0.0000305
16	0.0000219	0.0000073	0.0000292	0.0000153
17	0.0000000	0.0000000	0.0000000	0.0000076
18	0.0000000	0.0000073	0.0000073	0.0000038

Table 3. 0/1 Balance and Run Length Statistics of Code No. 3.

1/0 Balance = 0.4997/0.5003

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2549238	0.2547058	0.5096296	0.5000000
2	0.1230869	0.1235980	0.2466849	0.2500000
3	0.0623252	0.0613480	0.1236732	0.1250000
4	0.0304372	0.0307304	0.0611676	0.0625000
5	0.0148766	0.0151923	0.0300689	0.0312500
6	0.0069609	0.0073518	0.0143128	0.0156250
7	0.0037812	0.0035030	0.0072842	0.0078125
8	0.0018116	0.0017665	0.0035782	0.0039063
9	0.0009096	0.0008570	0.0017665	0.0019531
10	0.0005187	0.0004435	0.0009622	0.0009766
11	0.0001879	0.0003007	0.0004886	0.0004883
12	0.0000827	0.0000902	0.0001729	0.0002441
13	0.0000451	0.0000451	0.0000902	0.0001221
14	0.0000150	0.0000376	0.0000526	0.0000610
15	0.0000000	0.0000000	0.0000000	0.0000305
16	0.0000301	0.0000000	0.0000301	0.0000153
17	0.0000000	0.0000150	0.0000150	0.0000076
18	0.0000075	0.0000075	0.0000150	0.0000038
19	0.0000000	0.0000075	0.0000075	0.0000019

Table 4. 0/1 Balance and Run Length Statistics of Code No. 4

1/0 Balance = 0.5019/0.4981

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2367366	0.2388648	0.4756015	0.5000000
2	0.1258531	0.1247810	0.2506341	0.2500000
3	0.0649108	0.0650148	0.1299255	0.1250000
4	0.0348356	0.0348436	0.0696792	0.0625000
5	0.0178819	0.0176658	0.0355477	0.0312500
6	0.0092970	0.0091370	0.0184339	0.0156250
7	0.0048565	0.0044405	0.0092970	0.0078125
8	0.0028563	0.0024403	0.0052966	0.0039063
9	0.0013121	0.0012881	0.0026003	0.0019531
10	0.0006961	0.0008161	0.0015122	0.0009766
11	0.0003520	0.0004480	0.0008001	0.0004883
12	0.0001840	0.0001120	0.0002960	0.0002441
13	0.0000800	0.0000800	0.0001600	0.0001221
14	0.0000880	0.0000320	0.0001200	0.0000610
15	0.0000240	0.0000240	0.0000480	0.0000305
16	0.0000080	0.0000080	0.0000160	0.0000153
17	0.0000080	0.0000000	0.0000080	0.0000076
18	0.0000080	0.0000000	0.0000080	0.0000038
19	0.0000080	0.0000000	0.0000080	0.0000019
20	0.0000000	0.0000080	0.0000080	0.0000010

Table 5. 0/1 Balance and Run Length Statistics of Code No.5.

1/0 Balance = 0.4994/0.5006

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2458765	0.2454110	0.4912874	0.5000000
2	0.1261114	0.1246140	0.2507254	0.2500000
3	0.0627803	0.0640061	0.1267864	0.1250000
4	0.0315220	0.0326625	0.0641845	0.0625000
5	0.0166571	0.0165252	0.0331823	0.0312500
6	0.0084566	0.0081152	0.0165718	0.0156250
7	0.0043679	0.0021723	0.0041740	0.0039063
9	0.0011637	0.0010784	0.0022422	0.0019531
10	0.0004655	0.0006672	0.0011327	0.0009766
11	0.0002327	0.0002405	0.0004733	0.0004883
12	0.0001784	0.0001086	0.0002871	0.0002441
13	0.0000621	0.0000698	0.0001319	0.0001221
14	0.0000543	0.0000310	0.0000853	0.0000610
15	0.0000310	0.0000155	0.0000465	0.0000305
16	0.0000155	0.0000000	0.0000155	0.0000153
17	0.0000233	0.0000078	0.0000310	0.0000076
18	0.0000000	0.0000078	0.0000078	0.0000038
19	0.0000000	0.0000078	0.0000078	0.0000019

Table 6. 1/0 Balance and Run Length Statistics of Code No. 6

1/0 Balance = 0.4993/0.5007

Run Length	Consecutive 1-Bit	Consecutive 0-Bit	Total	Ideal
1	0.2528581	0.2530915	0.5059496	0.5000000
2	0.1255893	0.1238044	0.2493937	0.2500000
3	0.0617478	0.0628323	0.1245801	0.1250000
4	0.0308626	0.0308852	0.0617478	0.0625000
5	0.0146782	0.0149041	0.0295823	0.0312500
6	0.0072374	0.0073655	0.0146029	0.0156250
7	0.0034944	0.0035095	0.0070040	0.0078125
8	0.0018376	0.0017849	0.0036225	0.0039063
9	0.0007983	0.0009640	0.0017623	0.0019531
10	0.0004820	0.0004067	0.0008887	0.0009766
11	0.0002109	0.0002184	0.0004293	0.0004883
12	0.0000904	0.0000678	0.0001582	0.0002441
13	0.0000377	0.0000979	0.0001356	0.0001221
14	0.0000602	0.0000226	0.0000828	0.0000610
15	0.0000000	0.0000301	0.0000301	0.0000305
16	0.0000151	0.0000075	0.0000226	0.0000153
17	0.0000000	0.0000075	0.0000075	0.0000016

3.7.6 Auto-Correlation Functions of the Sequences

The auto-correlations of the code sequences described in Section 3.7.2 have been computed for a code phase shift over the entire length of each of the code sequence. FIGURE 85. is an example of the auto-correlation of the Code No. 1 sequence versus code phase shift, for a shift between 0 and 500 with the correlation window equal to 512. The auto-correlation function has a value of 1 at zero shift and near zero for all other shifts. The small value of correlation at non-zero code shift positions is highly desirable in order to have an accurate synchronization of the code at the receiver for a spread spectrum communication system. As a matter of fact, one would expect that the values of the correlation to approach zero value for any non-zero code chip shift position when the correlation window is increased to infinity. Indeed as is shown in FIGURE 86. the auto-correlation has much smaller values for non-zero code chip shift positions with a correlation window of 16,384 chips as compared to that with a window of 512 chips.

FIGURE 87. and FIGURE 88. represent the auto-correlation of Code No. 3 generated by the 4-DPLL system, for code phase shifts between zero and five hundred chips. FIGURE 87. has a correlation window of 512 and FIGURE 88. has a correlation window 16,384 code chip. They exhibit the same characteristics as those of the Code No.1 generated from the 2-DPLL system.

The histograms of the auto-correlation for the entire code phase shift positions, excluding the 0 shift point, have been obtained for all the code sequences given in Section 3.7.4. Shown in FIGURE 89. and FIGURE 90. are the histograms for the Codes No.1 and No. 3,

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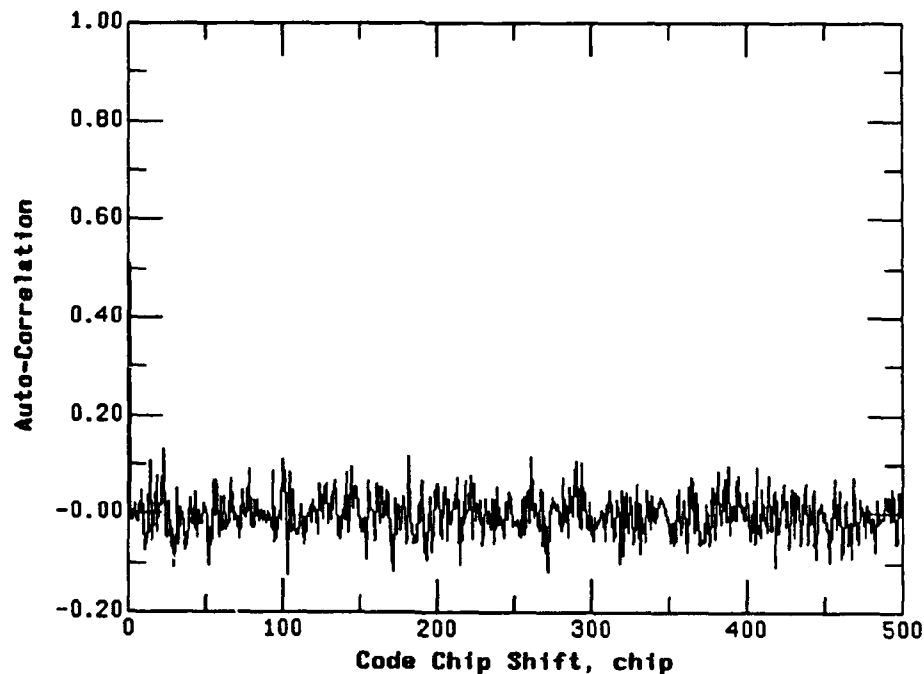


FIGURE 85. The Auto-Correlation Function Vs. Code Phase Shift of the Code No. 1. [Correlation window = 512 code chips

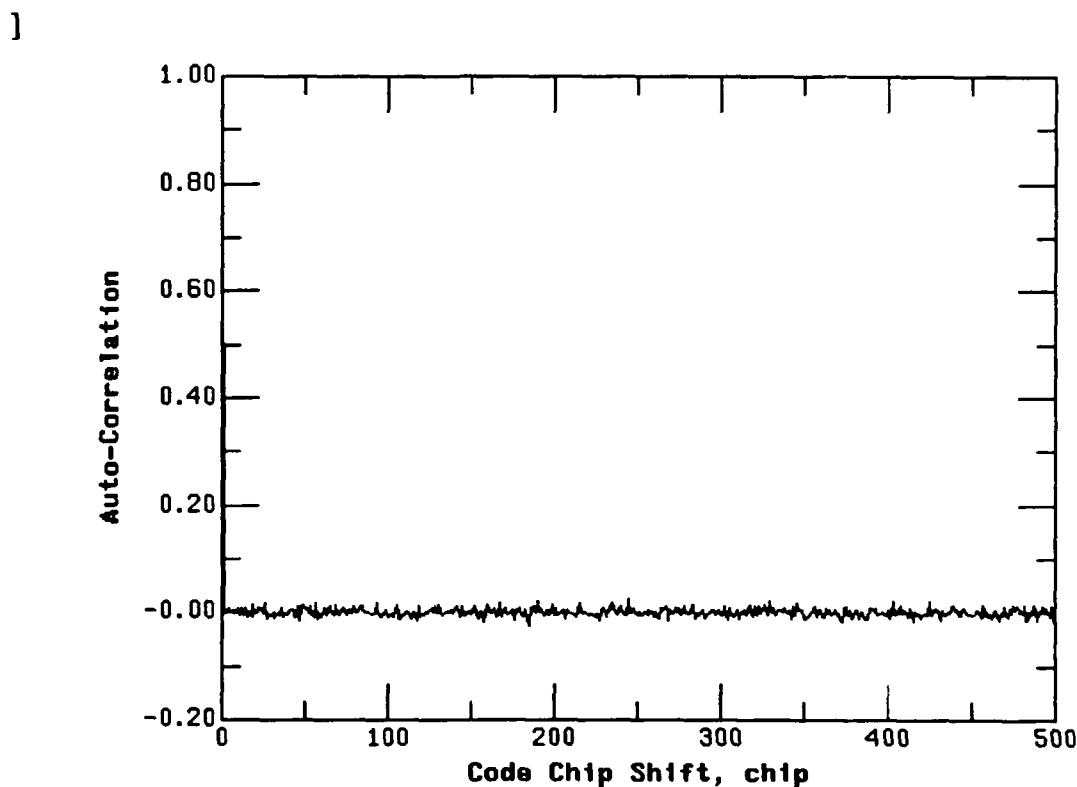


FIGURE 86. The Auto-Correlation Function Vs. Code Phase Shift of the CODE No.1. [Correlation Window = 16,384 code chips.

for correlation windows of 512, and 16,384 code chips. It can be seen that the mean value of the correlation is approximately equal to zero, and that the variance decreases as the correlation window is increased. It is also found that the absolute maximum value of the correlation is less than 0.2 for the correlation window of 512 code chips and decreases to less than 0.05 for the cases where the window is 16,384 code chips

Table 7 gives the standard deviation of the auto-correlation functions for all of the six (6) code sequences listed in Section 3.7.4, for the correlation windows of 512, 2,048, and 16,384 code chips. It is seen that the standard deviation is inversely proportional to the square-root of the correlation window.

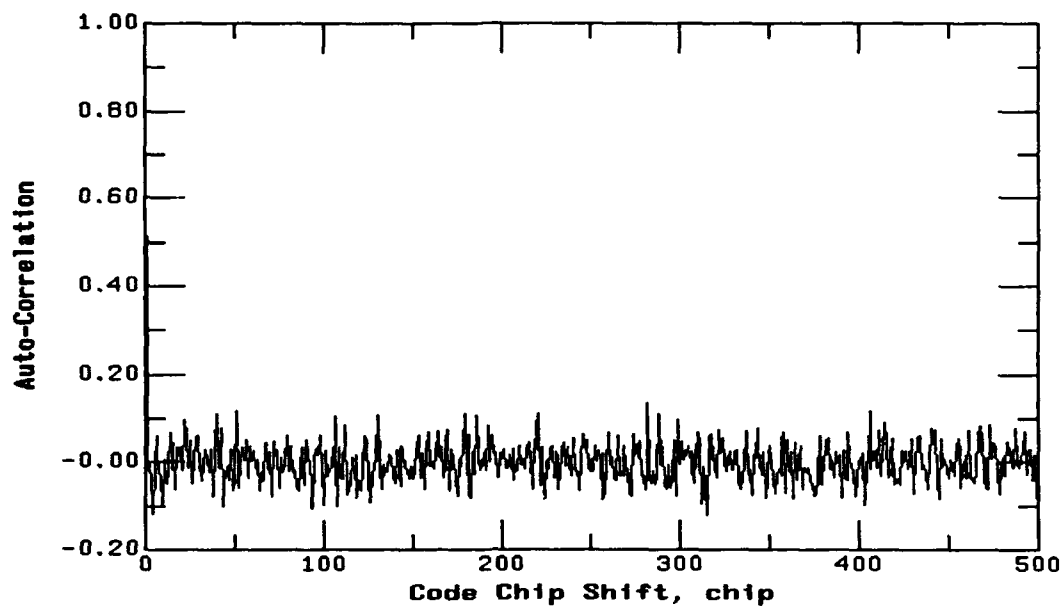


FIGURE 87. The Auto-Correlation Function Vs. Code Phase Shift of the Code No. 3. [Correlation Window = 512 code chips.

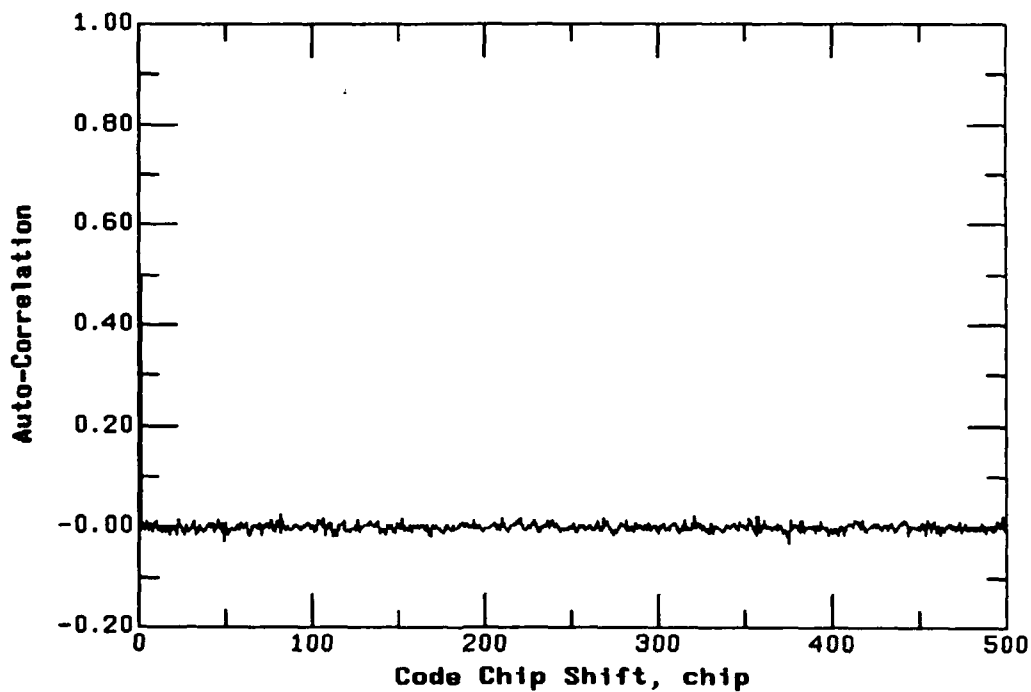


FIGURE 88. The Auto-Correlation Function Vs. Code Phase Shift of the Code No.3. [Correlation Window = 16,384 code chips

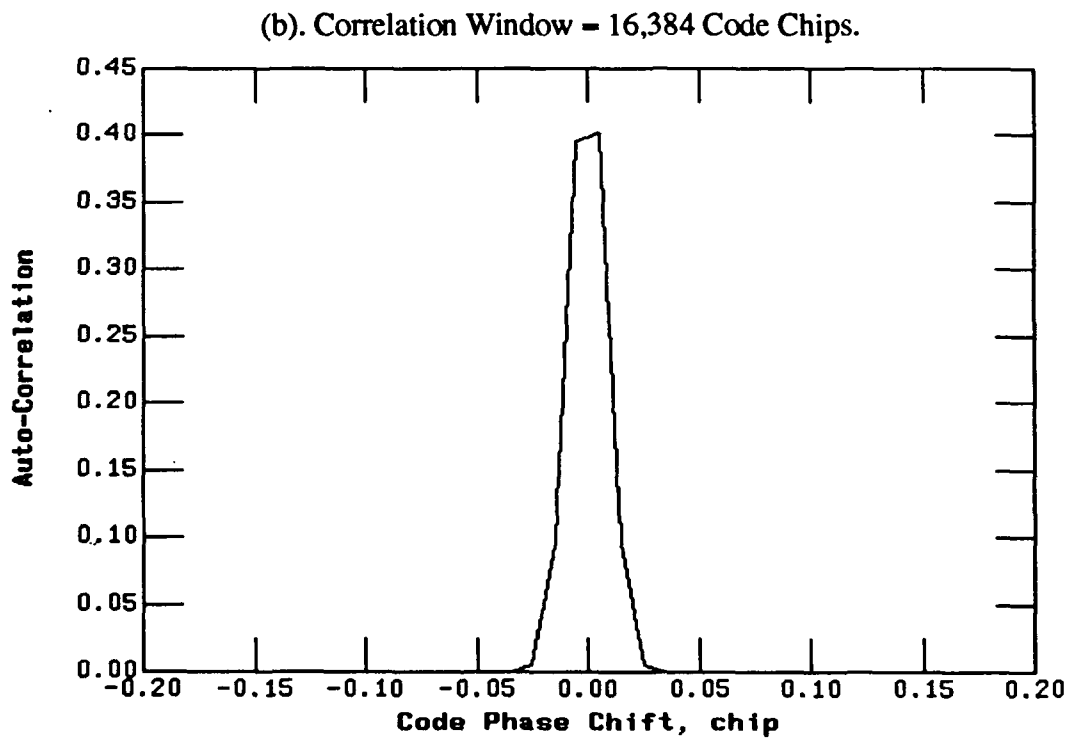
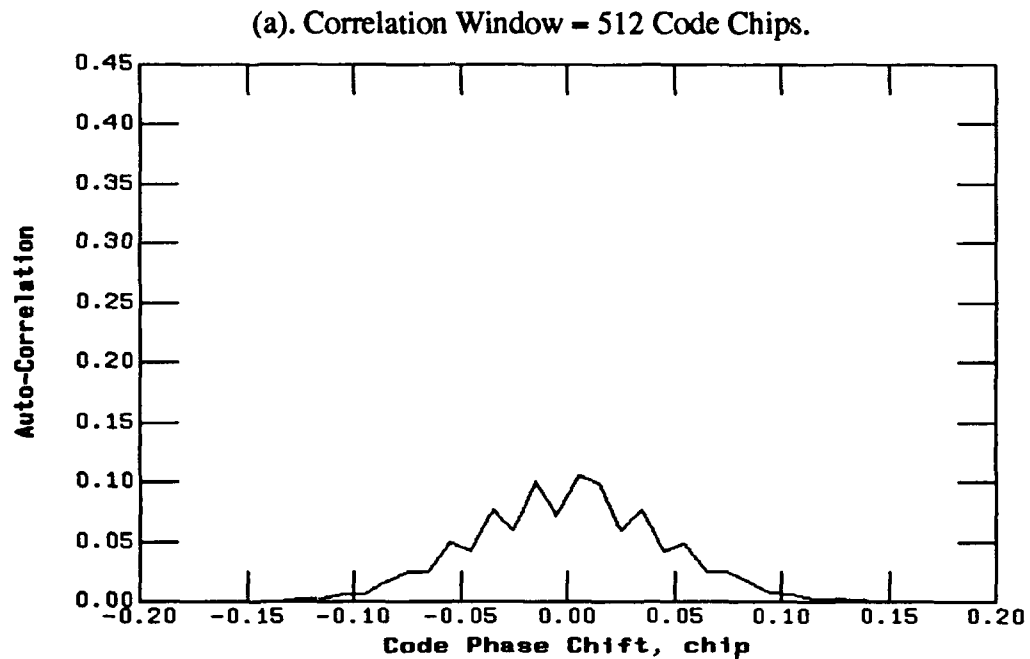
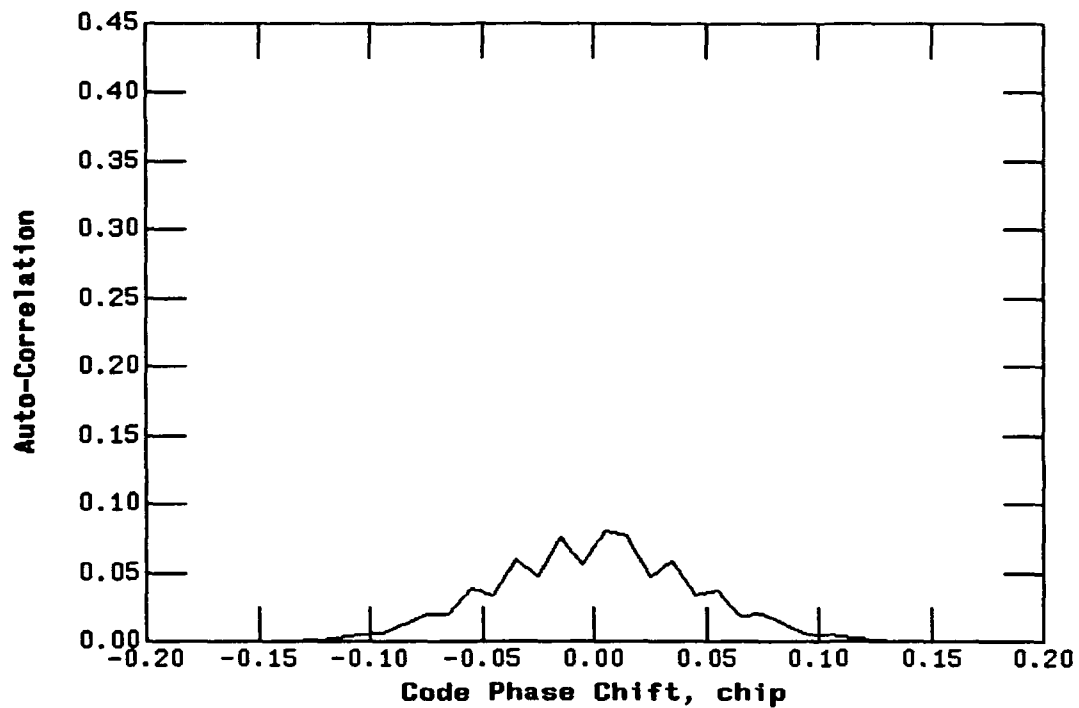


FIGURE 89. The Histogram of the Auto-Correlation Function of the Code No. 1

(a). Correlation Window = 512 Code Chips.



(b). Correlation Window = 16,384 Code Chips.

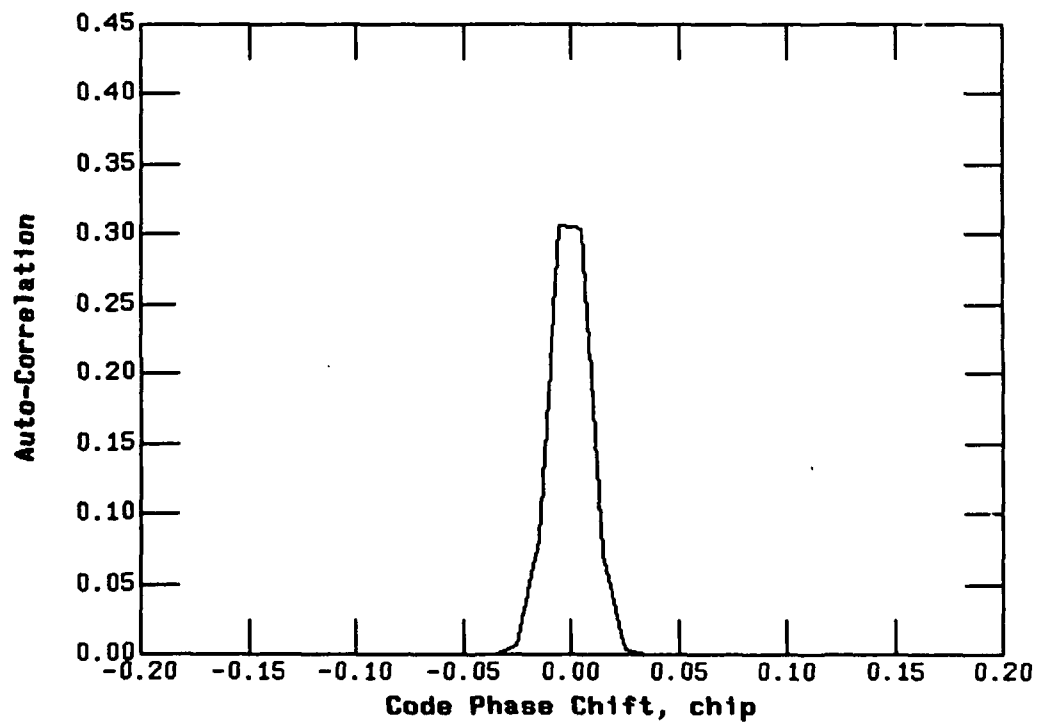


FIGURE 90. The Histogram of the Auto-Correlation of the Code No.3

Table 7. Standard Deviation of the Auto-Correlation of the Code Sequences
(Excludes the zero phase shift point.)

Code	Correlation Window (number of code chips)		
	512	2,048	16,384
Code No. 1	4.41×10^{-2}	2.23×10^{-2}	8.35×10^{-3}
Code No. 2	4.42×10^{-2}	2.23×10^{-2}	8.39×10^{-3}
Code No. 3	3.90×10^{-2}	1.97×10^{-2}	7.51×10^{-3}
Code No. 4	4.45×10^{-2}	2.24×10^{-2}	7.57×10^{-3}
Code No. 5	4.43×10^{-2}	2.23×10^{-2}	8.32×10^{-3}
Code No. 6	4.45×10^{-2}	2.22×10^{-2}	7.80×10^{-3}

NOTE: The mean values for all the code are less than 2×10^{-4} .

3.7.7 Cross-Correlation Between Two of The Code Sequences

The cross-correlations for several combinations of two of the six (6) code sequences listed in Section 3.7.4 were computed. Specifically, the cross-correlations for the following combinations of two code sequences have been investigated.

Case 1: Cross-correlation between Codes No. 1 and No. 2.

Case 2: Cross-correlation between Codes No. 1 and No. 3.

Case 3: Cross-correlation between Codes No. 3 and No. 4.

Case 4: Cross-correlation between Codes No. 3 and No. 5.

Case 5: Cross-correlation between Codes No. 3 and No. 6.

Case 6: Cross-correlation between Codes No. 4 and No. 5.

Case 7: Cross-correlation between Codes No. 5 and No. 6.

The cross-correlation values at all code phase shift positions should, ideally, be very close to zero if they are to be useful for CDMA communications. FIGURE 91. through FIGURE 93. show the cross-correlations vs. code phase shift for Cases 1 through 3 listed above, where the code phase shift was from 0 to 500. It is seen that the absolute values of the cross-correlation are small for all code chip shift positions, and they become smaller as the correlation window is increased.

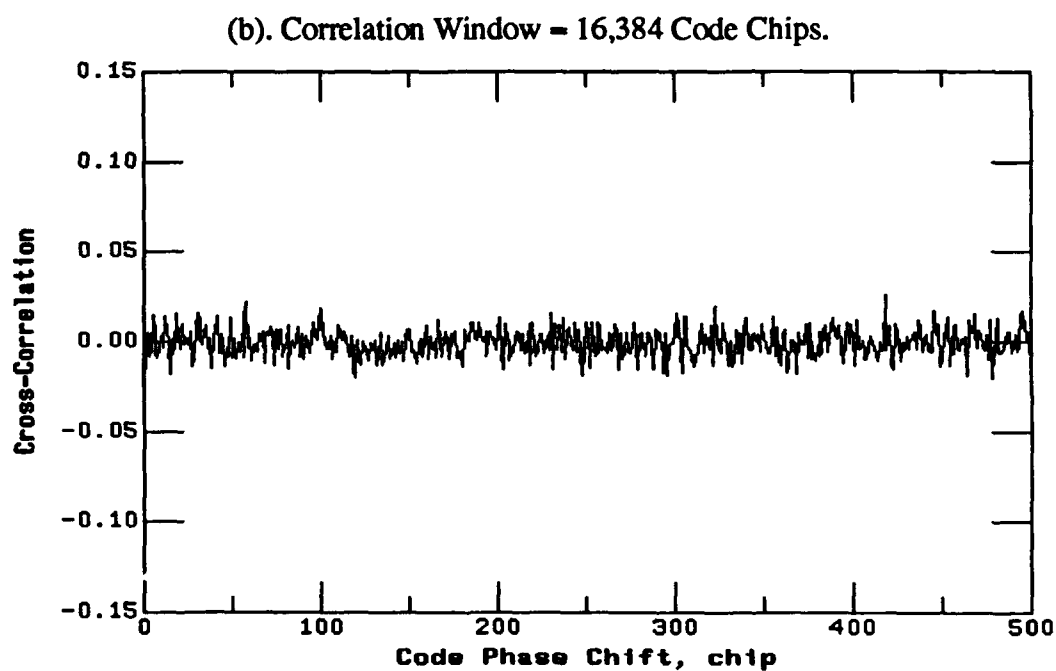
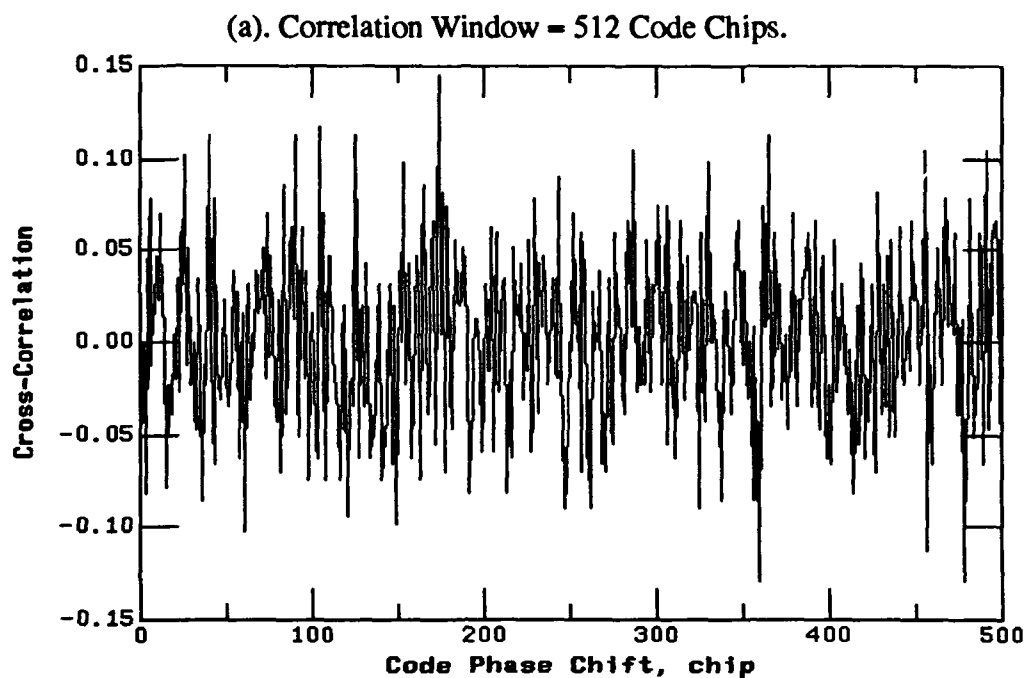
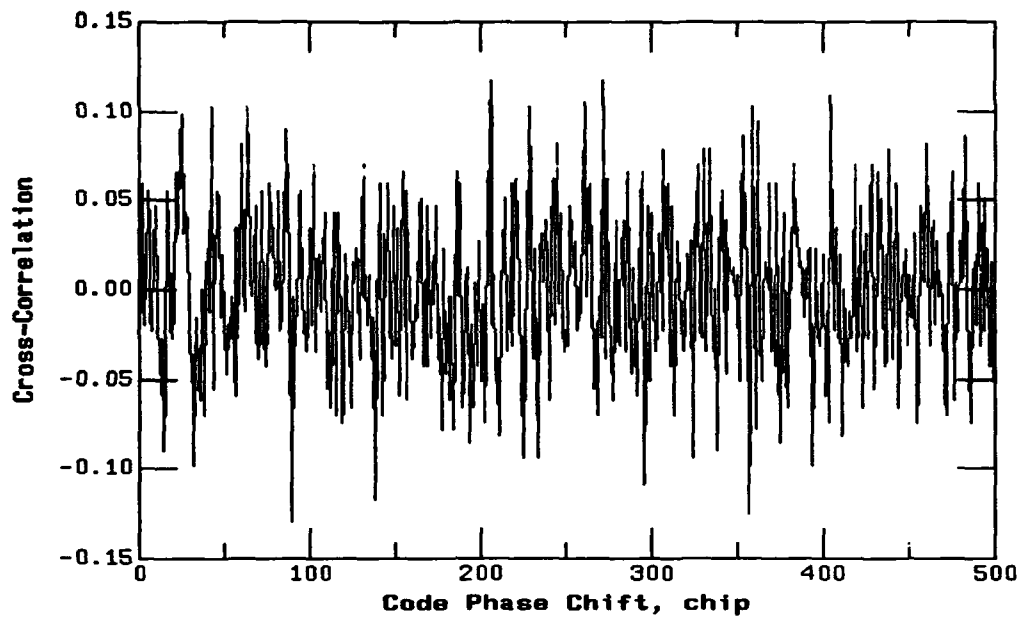


FIGURE 91. The Cross-Correlation Function Vs. Code Phase Shift for the Code Sequences No.1 and No.2. [Case 1.]

(a). Correlation Window = 512 Code Chips.



(b). Correlation Window = 16,384 Code Chips.

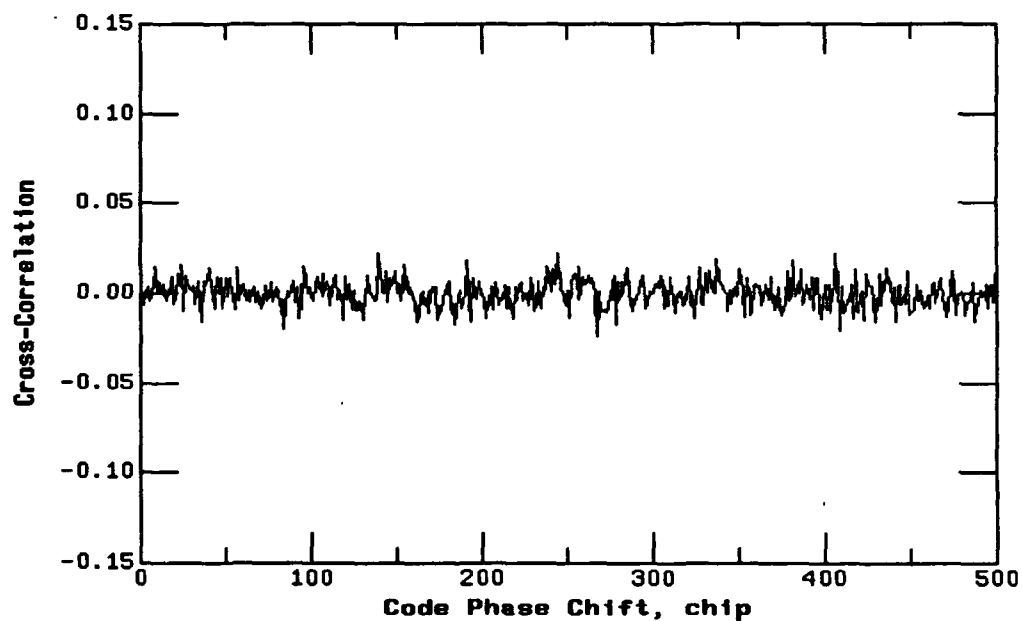
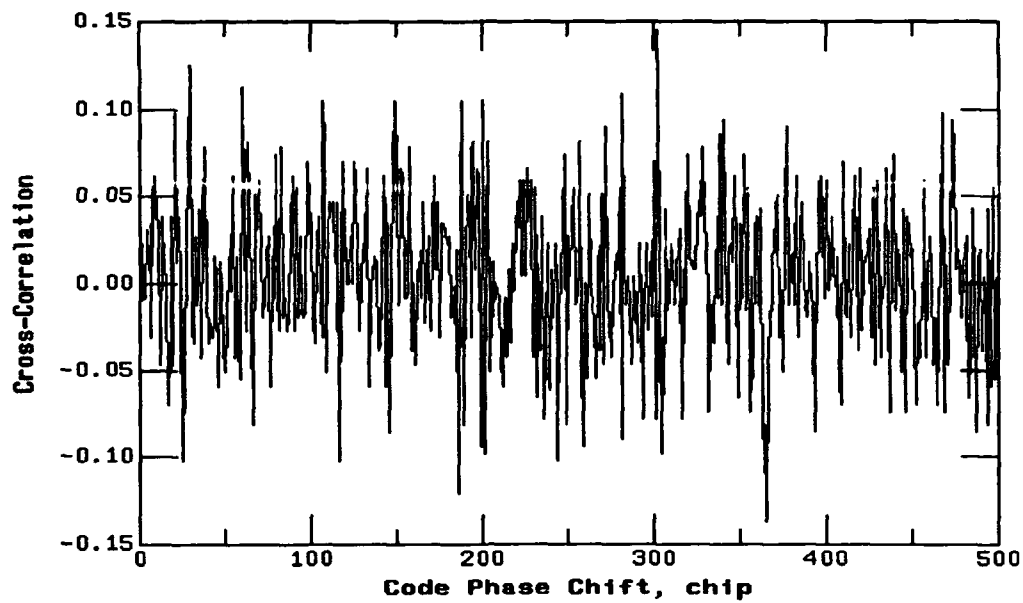


FIGURE 92. The Cross-Correlation Function Vs. Code Phase Shift of the Code Sequences No. 1 and No.3. [Case 2.]

(a). Correlation Window = 512 Code Chips.



(b). Correlation Window = 16,384 Code Chips.

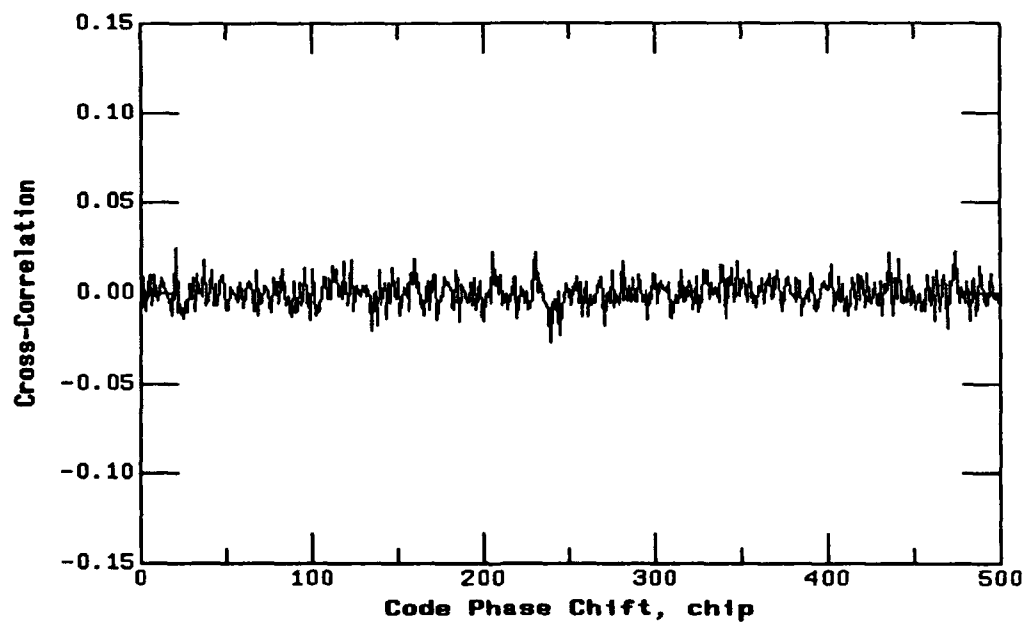
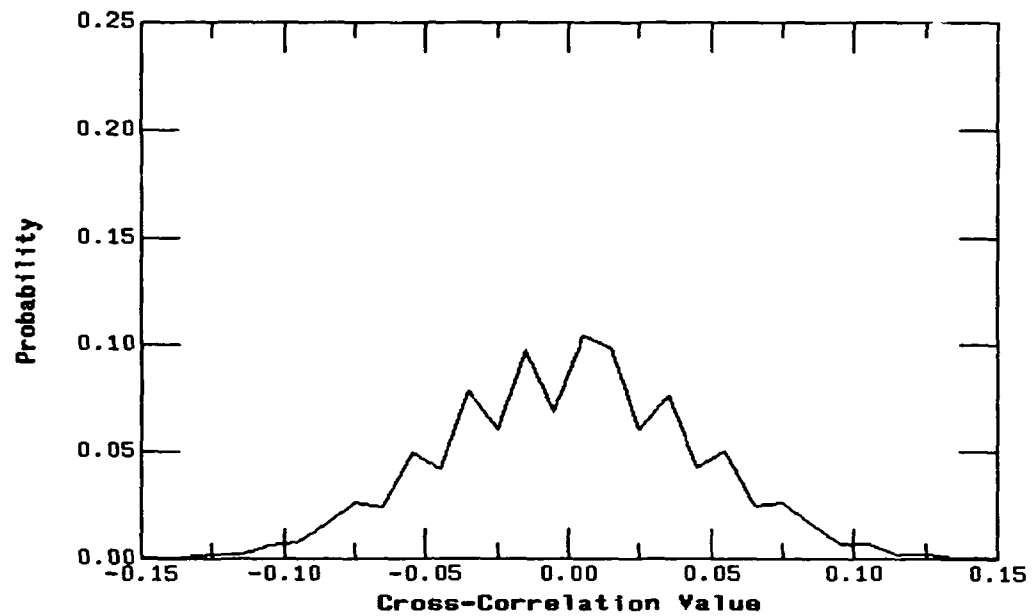
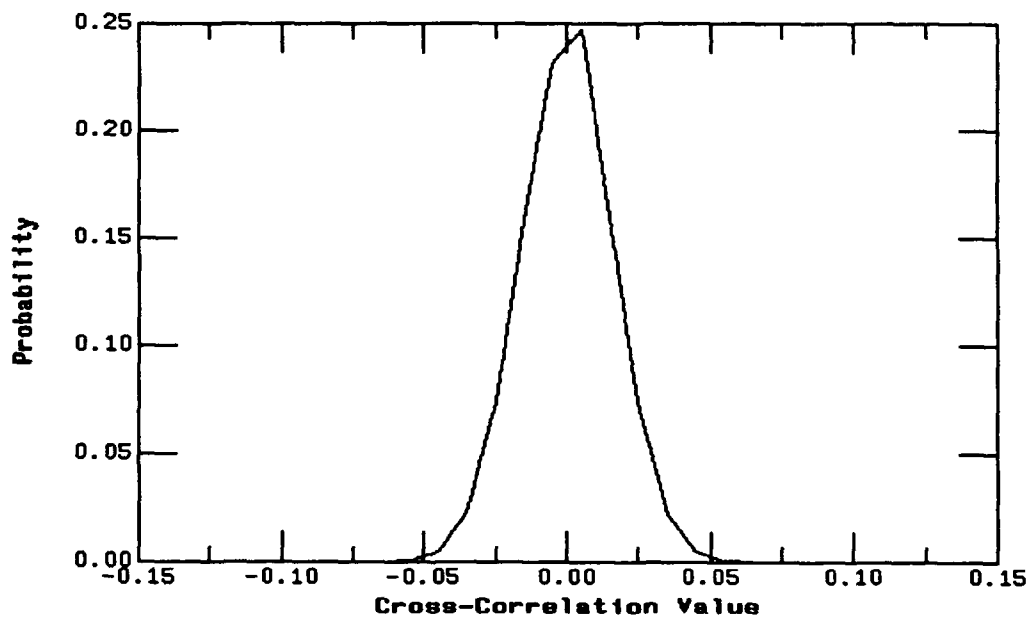


FIGURE 93. The Cross-Correlation Function Vs. Code Phase Shift of the Code Sequences No. 3 and No.4. [Case 3.]

(a). Correlation Window = 512 Code Chips.

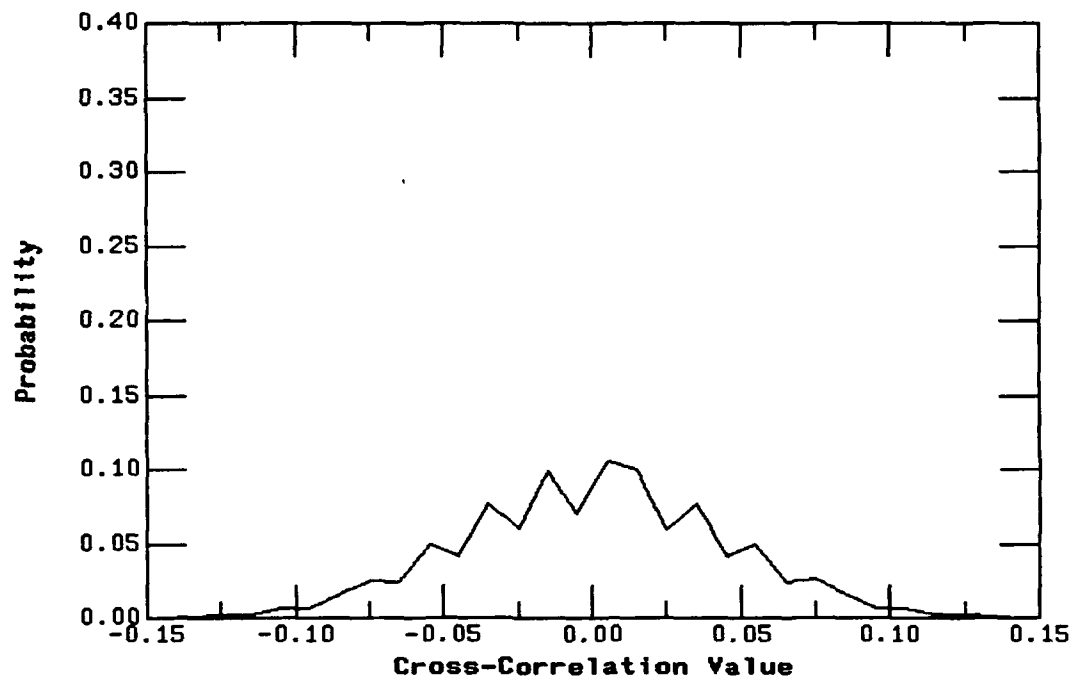


(b). Correlation Window = 16,384 Code Chips.

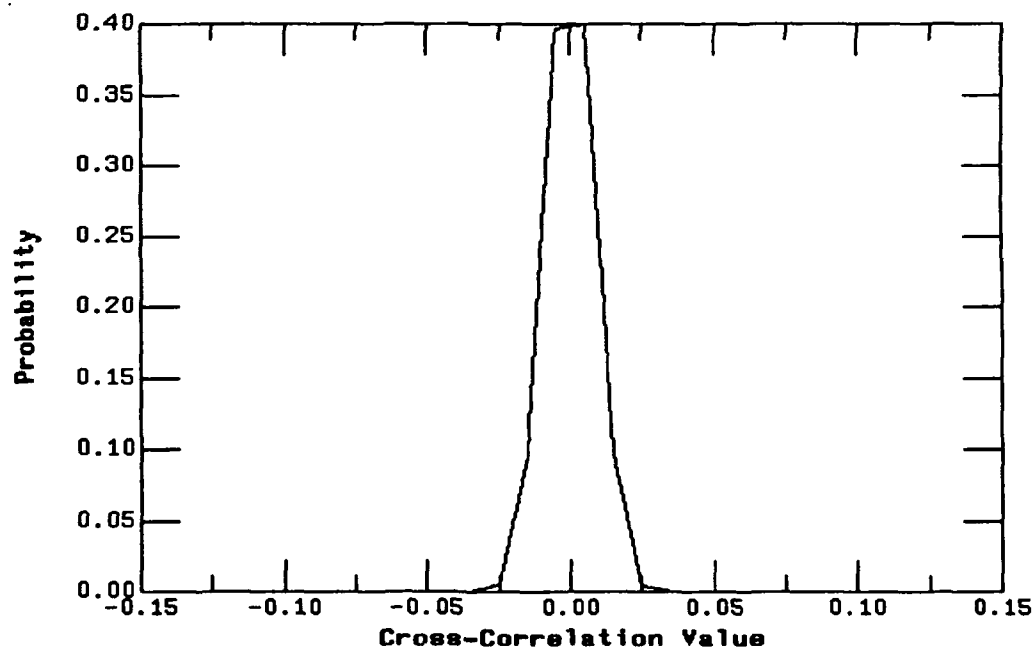


**FIGURE 94. The Histogram of the Cross-Correlation Function of the Code Sequences No.1 and No.2.
[Case 1.]**

(a). Correlation Window = 512 Code Chips.

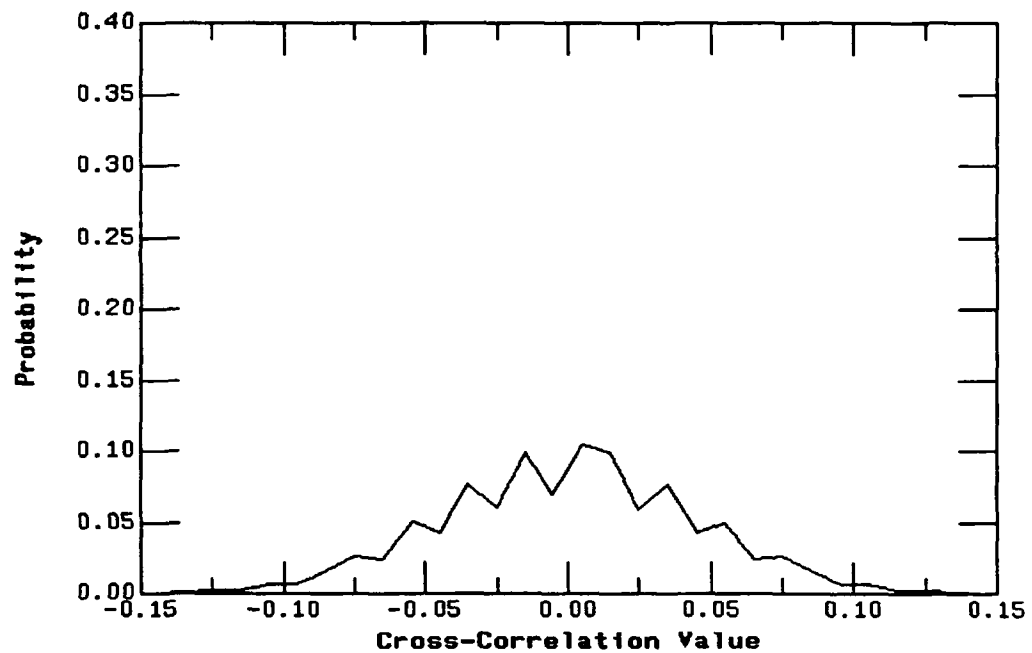


(b). Correlation Window = 16,384 Code Chips



**FIGURE 95. The Histogram of the Cross-Correlation Function of the Code Sequences No. 1 and No3.
[Case 2.]**

(a). Correlation Window = 512 Code Chips.



(b). Correlation Window = 16,384 Code Chips.

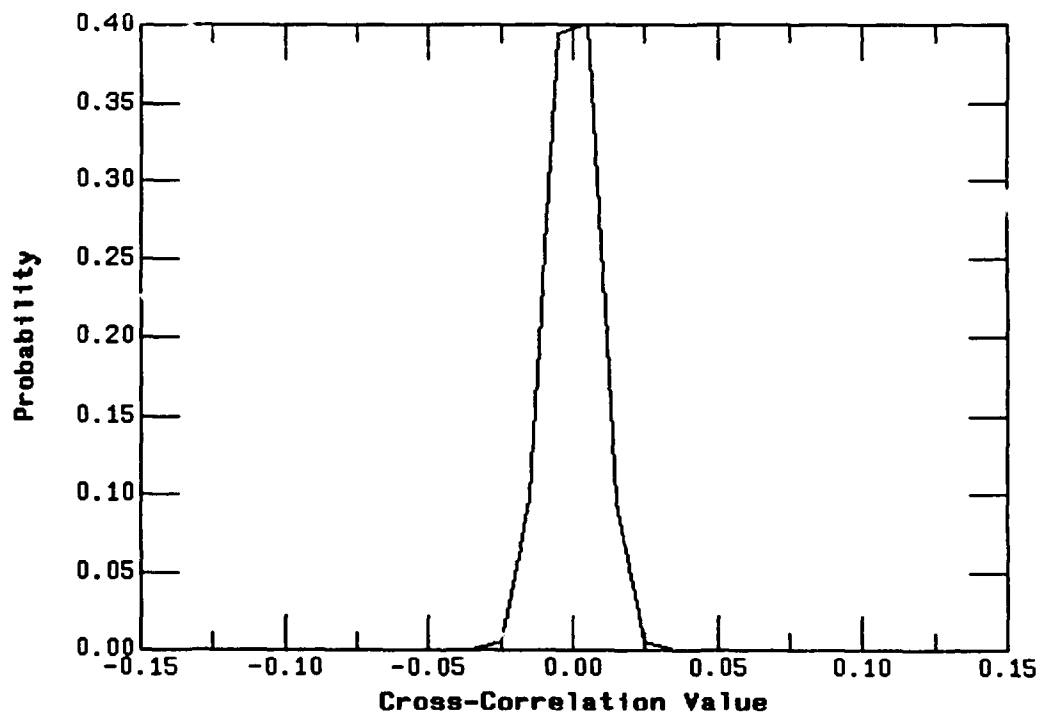


FIGURE 96. The Histogram of the Cross-Correlation Function of the Code Sequences No. 3 and No.4. [Case 3.]

As stated above, one of the many requirements for a set of PN codes to be useful in a code division multiple access (CDMA) communication system is that the cross-correlation between any two (2) codes of the set must remain small for all code shift positions. To demonstrate that such is the case for code sequences generated using the non-linear systems of coupled DPLLs, the histograms for the cross-correlations of the seven cases listed above have been obtained. They are shown in FIGURE 94. through FIGURE 96. It is seen that the mean values of the cross-correlation are nearly zero for all cases, and the spread of the histogram decreases as the correlation window is increased. Hence, one would expect that the RMS value of the cross-correlation of any two code sequences approaches zero as the correlation window is extended to infinity. It is also seen that these histograms have remarkably similar characteristics for all cases investigated.

Table 8 gives the standard deviations of the cross-correlations of the six (6) cases listed at the beginning of this section. Again, it is seen that the standard deviation is inversely proportional to the square-root of the correlation window.

Table 8. The Standard Deviation of the Cross-Correlations of Two Code Sequences

Codes	Correlation Window (number of chips)		
	512	2,048	16,384
Codes No. 1 and No. 2	6.85×10^{-3}	3.44×10^{-3}	2.46×10^{-3}
Codes No. 1 and No. 3	4.40×10^{-2}	2.21×10^{-2}	7.80×10^{-3}
Codes No. 3 and No. 4	7.00×10^{-3}	3.75×10^{-3}	2.00×10^{-3}
Codes No. 3 and No. 5	4.41×10^{-2}	2.24×10^{-2}	8.33×10^{-3}
Codes No. 3 and No. 6	4.41×10^{-2}	2.24×10^{-2}	8.35×10^{-3}
Codes No. 4 and No. 5	6.82×10^{-3}	3.43×10^{-3}	1.29×10^{-3}
Codes No. 5 and No. 6	6.82×10^{-3}	3.34×10^{-3}	1.28×10^{-3}

NOTE: The mean values of the cross-correlations for all cases are less than 10^{-4}

3.7.8 Acquisition Behavior of the Code Sequences

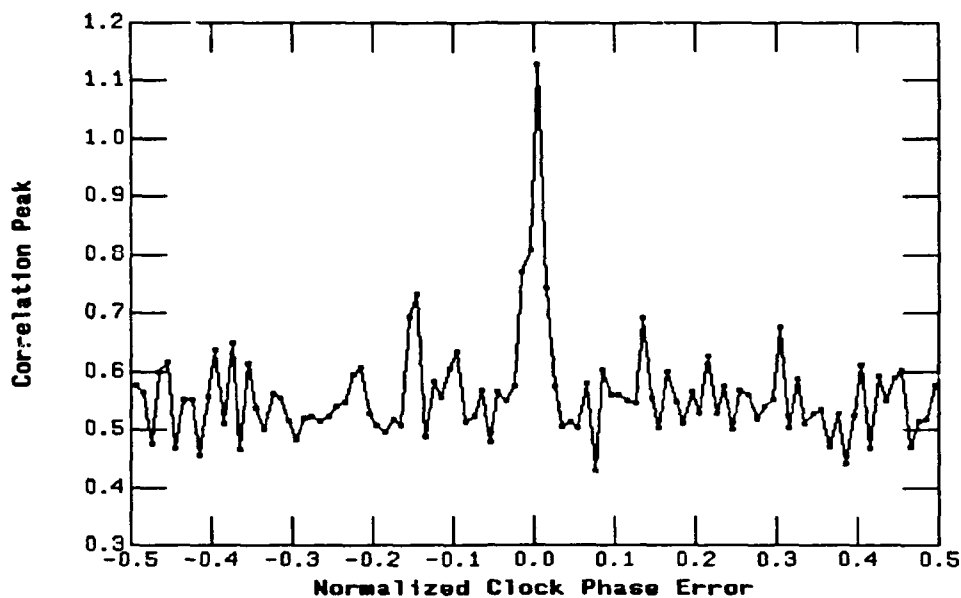
Simulations of the clock and code phase acquisitions under noisy conditions have been performed using the Monte Carlo method. In the simulation, the code phases of the received code sequence and the regenerated sequence at the receiver are initially set to be off by an arbitrary number of code chips, and the clock phases of the transmitter and the receiver are off by as much as one-half of the clock period.

The acquisition algorithm described in Section 3.7.3 is used in the simulation. During the acquisition phase the transmitted sequence of a fixed number code chips is continuously repeated. During the first pass of attempting to establish the required synchronizations, the

clock phase of the receiver is gradually stepped by an increment equal to a small fraction of the clock period. For each of the clock phases the code sequence generated by the receiver was correlated with the received sequence from the transmitter simultaneously for all the different code phases, using as many correlators as there were code chips to be correlated. The code phase and clock phase synchronizations were declared to have been achieved whenever the correlation peak at a given clock phase position exceeded 0.99. In the case where the maximum value of the correlation peak remained less than 0.99 after the clock phase has been shifted for one clock period, the second phase of the acquisition process was initiated. This was done by searching the clock phase with an time increment equal to one-tenth of the original increment. The search was performed in the vicinity of the clock phase position at which the maximum value of a correlation peak had been observed during the first phase of the search. It has been found that synchronization can be achieved within the first three (3) passes with an input signal-to-noise ration (SNR) of -12 dB or higher.

Given below are correlation peaks versus the clock phase errors during the processes of code phase and clock phase acquisitions. FIGURE 97. is for the Code No.1 using a correlation window of 512 code chips. Part a is for code generated from the output of the second DPLL and part b is for the code generated from the output of the first DPLL. The code sequence is acquired in one pass for both cases. FIGURE 98. and FIGURE 99. are for the same case except that the correlation window is 1,024 code chips. The codes generated from the output of the second as well as the first DPLL are acquired in two passes. The reason multiple passes are needed to acquire the codes is that a slight off-set in the clock phase will cause many code chip mismatches when correlation window is widened.

(a). Code Generated From the Output of the Second DPLL.



(b). Code Generated From the Output of the First DPLL.

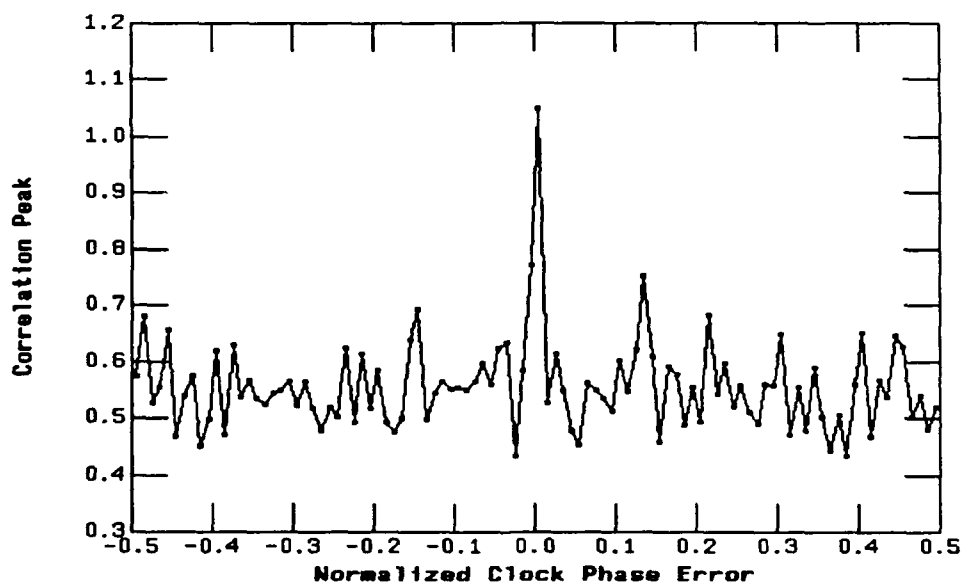
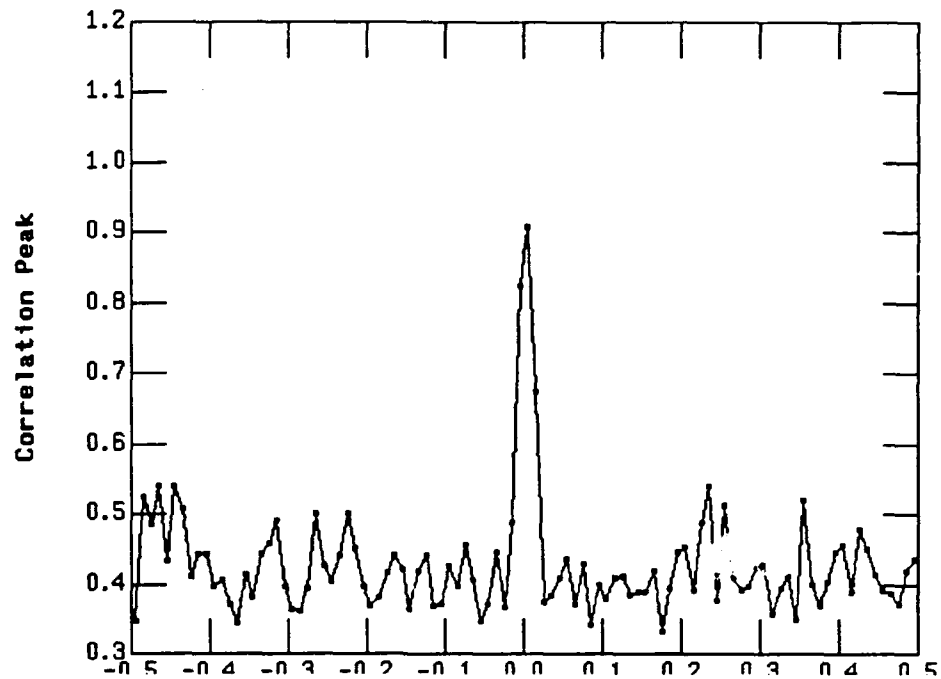


FIGURE 97. Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No.1 with correlation window of 512 code chips.

(a). Code Generated From the Output of the Second DPLL - First Pass.



(b). Code Generated From the Output of the Second DPLL - Second Pass.

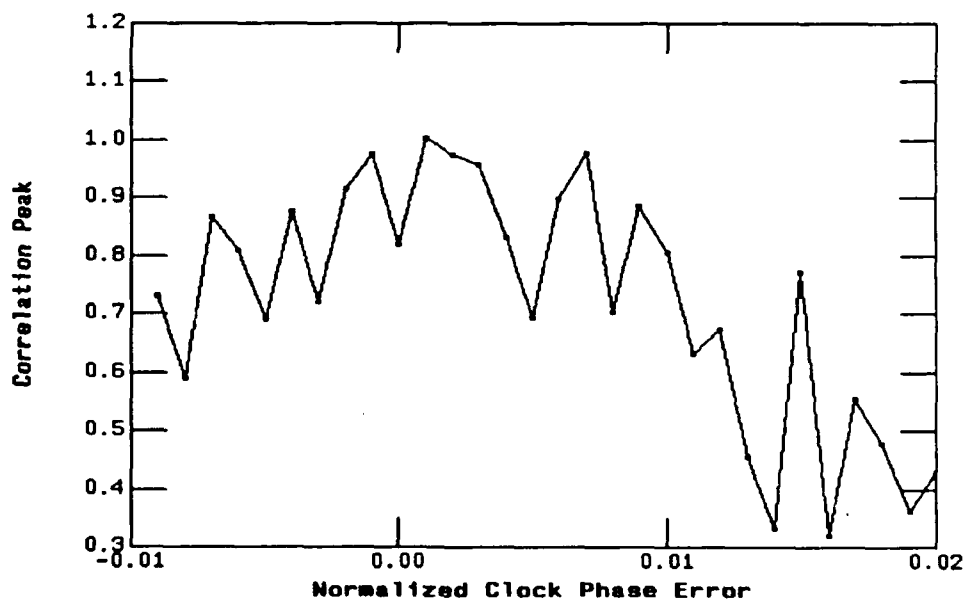
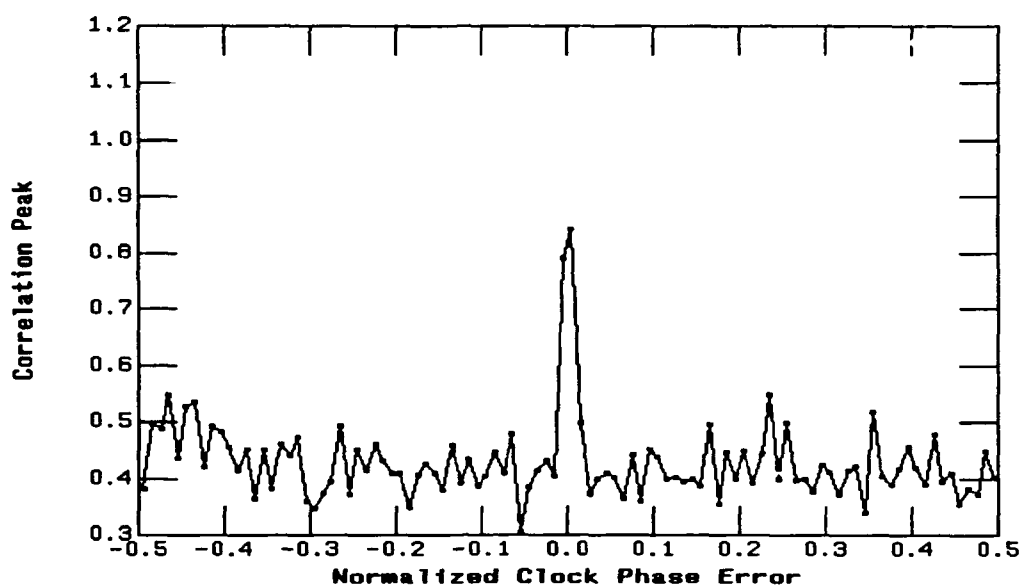


FIGURE 98. The Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 1 With Correlation Window of 1,024 Code Chips

(a). Code Generated From the Output of the First DPLL - First pass.



(b). Code Generated From the Output of the First DPLL - Second Pass.

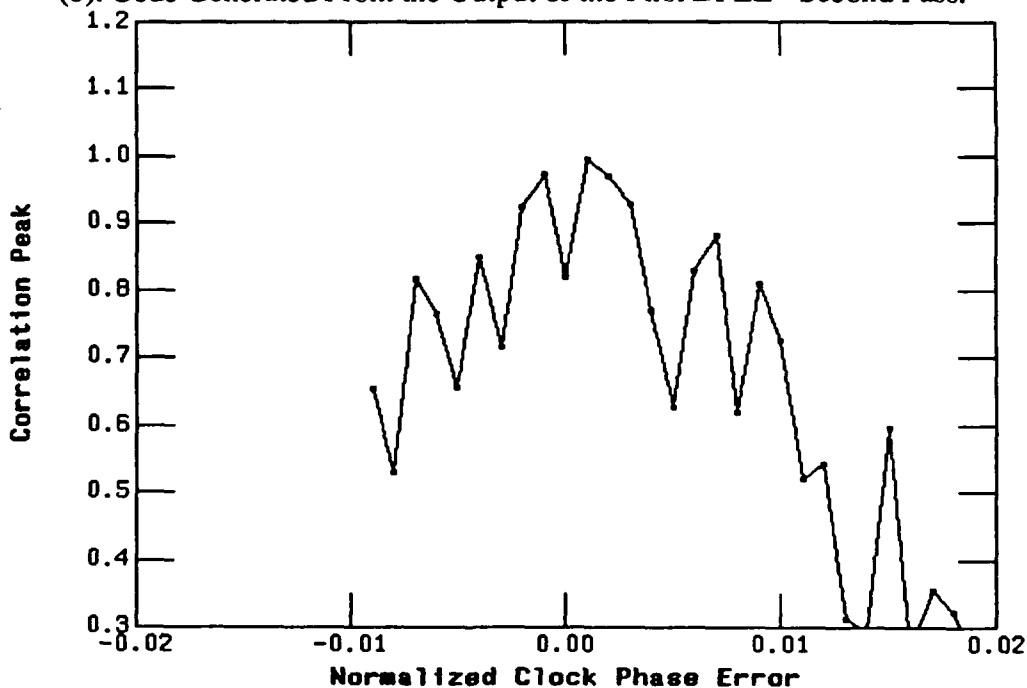
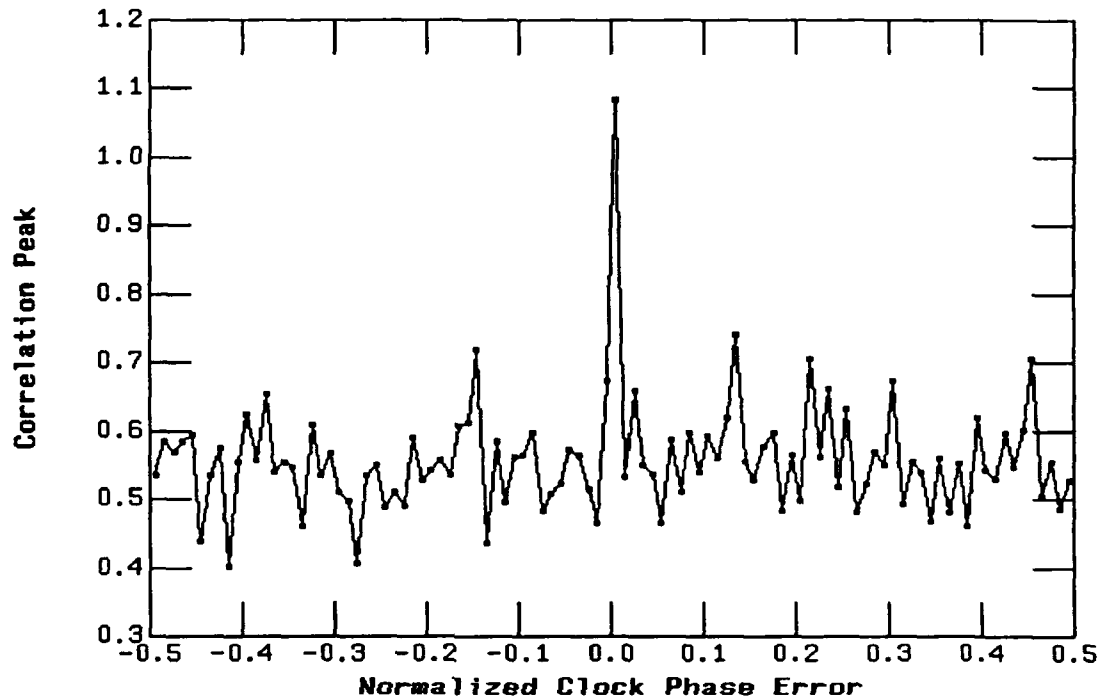


FIGURE 99. The Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 1 With Correlation Window of 1,024 Code Chips

FIGURE 100. is a graph of the correlation peaks versus clock phase error during the acquisition of the Code No. 3 using a correlation window of 512 code chips. FIGURE 101. through FIGURE 103. depict the same thing with the correlation window of 1,024 code chips. Again, it is seen that multiple passes are required to acquire the codes when

the correlation window is 1,024 code chips, while one single pass is needed for the correlation window of 512 code chips.

(a). Code Generated From the Output of the Fourth DPLL.



(b). Code Generated From the Output of the Third DPLL.

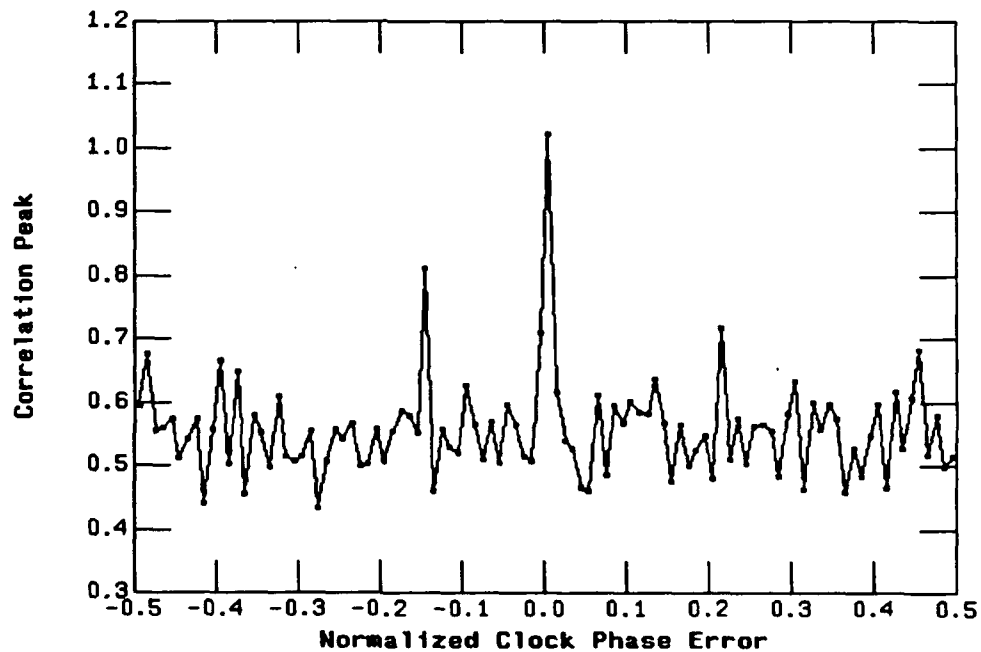
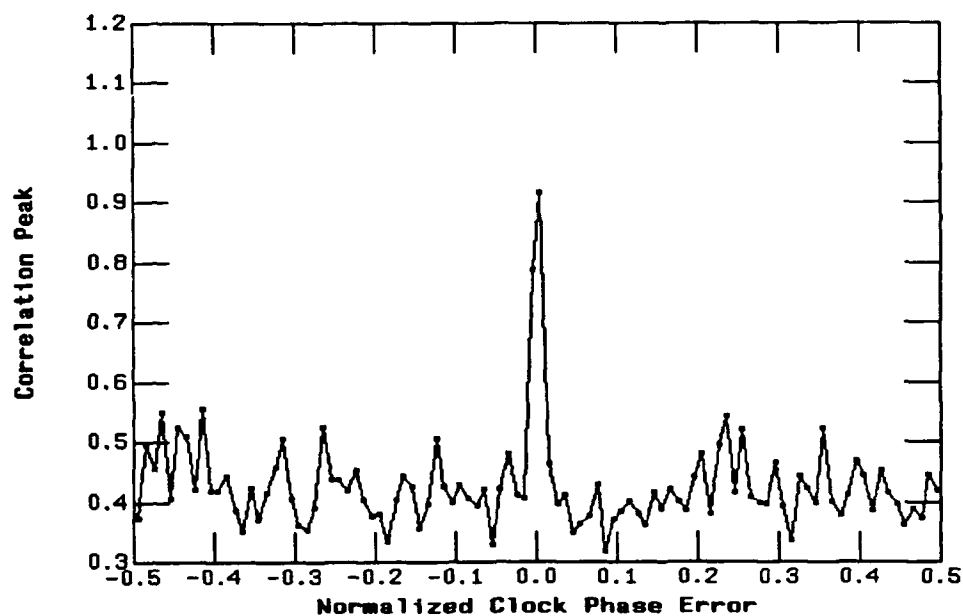


FIGURE 100. Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 3 With Correlation Window of 512 Code Chips.

(a.). Code Generated From the Output of the Fourth DPLL - First Pass.



(b). Code Generated From the Output of the Fourth DPLL - Second Pass.

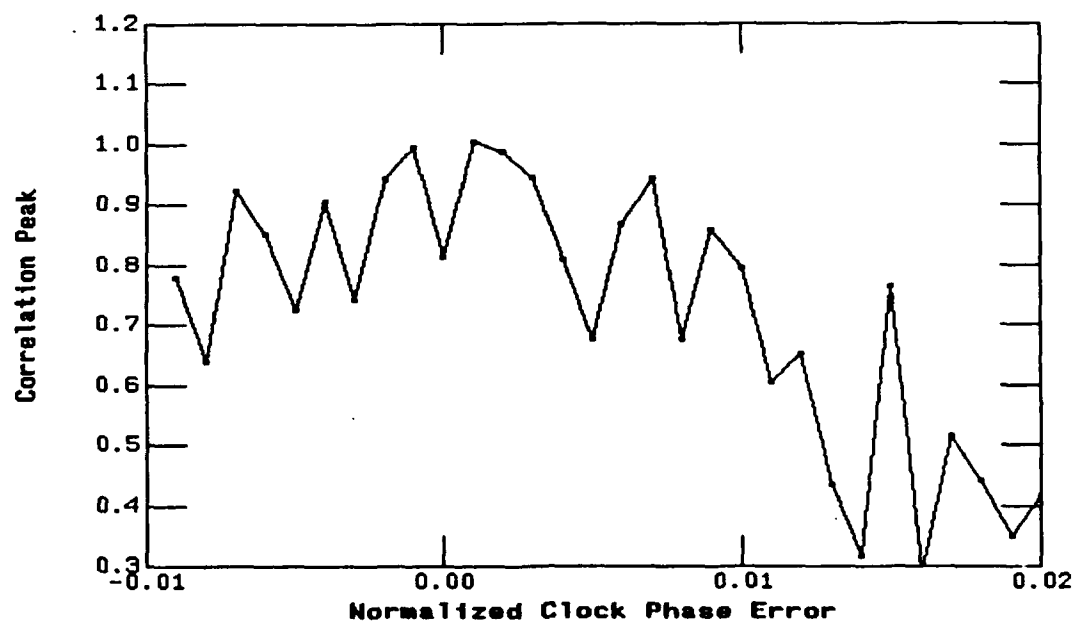
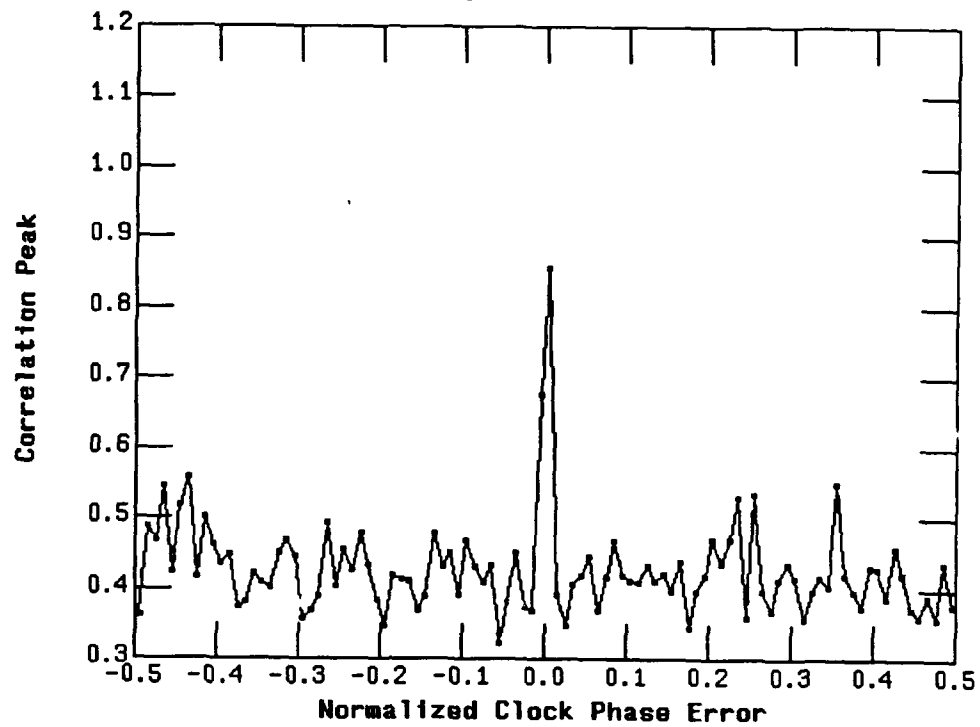


FIGURE 101. The Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 3 Using Correlation Window of 1,024 Code Chips

(a). Code generated From the Output of the Third DPLL - First Pass.



(b). Code Generated From the Output of the Third DPLL - Second Pass.

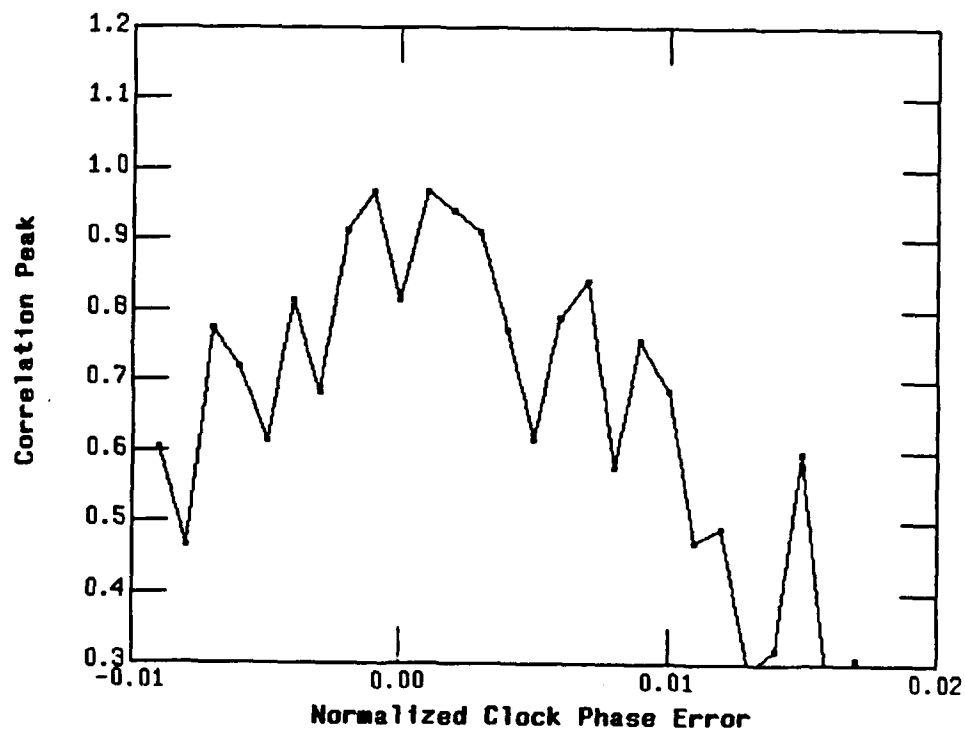


FIGURE 102. The Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 3 Using Correlation Window of 1,024 Code Chips}

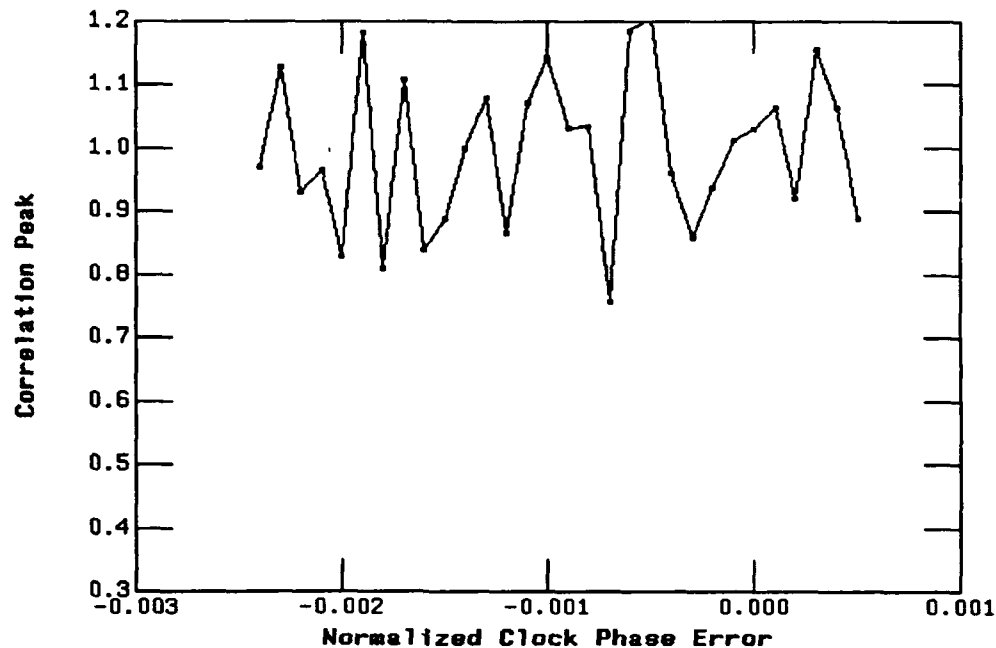


FIGURE 103. The Correlation Peak Vs. Clock Phase Error During the Acquisition of the Code No. 3 Using Correlation Window of 1,024 Code Chips Code Generated From the Output of the Third DPLL - Third Pass.

One Monte Carlo simulation was done to simulate the acquisition of a code sequence under noisy conditions. It would be necessary to carry out several hundred simulations in order to obtain the statistics (mean values and variances) of the number of passes required to acquire each of the codes starting from any arbitrary code phase off-set and clock phase error.

3.7.9 Conclusion

Code sequences generated from the 2-DPLL and 4-DPLL non-linear systems have been investigated to determine if they have the desired properties as outlined in Section 3.7.2. It has been found that the six code sequences investigated have all four (4) of the properties required. In addition, it has been found that those code sequences generated from the output of the DPLL having positive Lyapunov exponent have only one positive auto-correlation peak. This is a highly desirable property.

It has been found that code and clock phase synchronization can be achieved within one to three passes when the initial clock timing search increment is less than 1/100 of the clock period, and the input signal-to-noise ratio is equal to or higher than - 12 dB.

A larger collection of sequences generated using the system of FIGURE 67., with different numbers of DPLL's in the system and with different coupling coefficients matrices, need

to be studied so as to be certain that the codes sequences generated have the desired properties as given in Section 2.0. The question of the periodicities of these sequences must be addressed either through theoretical investigation or simulations. Ideally, the periods of the sequences generated by the system would be infinite. All the simulations were done using a digital computer with double precision arithmetic operations. The effects of using a shorter word length in the arithmetic operations on the properties of sequences being studied require further investigation.

3.7.10 References

1. S.W. Golomb. Shift Register Sequences, Holden-Day, Inc. 1967
2. J.K. Holmes, Coherent spread Spectrum Systems, John Wiley & Sons, 1982

3.8 Analogue Phase Lock Loop

This section contains a review of the work done on the analogue phase lock loop.

3.8.1 Overview

Phase locked loops (PLLs) are useful for phase and frequency, synchronization. An independent study at Ford Aerospace (now LORAL Aerospace) explored possibilities for high speed data recovery using an analogue phase lock loop which contained a hard limiter¹. A linear analysis indicated that such a loop showed great promise. However, since the behavior of a phase lock loop with a hard limiter in it was not well understood it was decided that an analysis of a system containing a hard limiter should be performed using the methods of non linear dynamics. In this section we present the results of that investigation.

3.8.2 System description

The system studied was a second order analogue phase lock loop² with the addition of an ideal limiter. The systems behavior was investigated for three different types of input; FM, BPSK, and square waves. The FM and BPSK assumed a sinusoidal carrier. FIGURE 104. is a representation of the loop.

Θ_i is the phase of the input signal, Θ_o is the phase of the VCO output, h is the output of the phase detector(PD). The output of the hard limiter is u_l and the output of the filter is u_f . The phase difference is given by:

$$\Phi(t) = \Theta_i - \Theta_o \quad (61)$$

The output of the limiter is either -1 if $h \leq 0$ or +1 if $h > 0$

The output of the filter is governed by its transfer function which is

$$\frac{1 + s\tau_2}{1 + s\tau_1} \quad (62)$$

where s is the operational variable and τ_1 and τ_2 characterize the filter. The output phase of the VCO is given by

$$\frac{d\Theta_o}{dt} = \omega_o + Ku_f \quad (63)$$

where ω_0 is the free running frequency of the VCO and K is its gain.

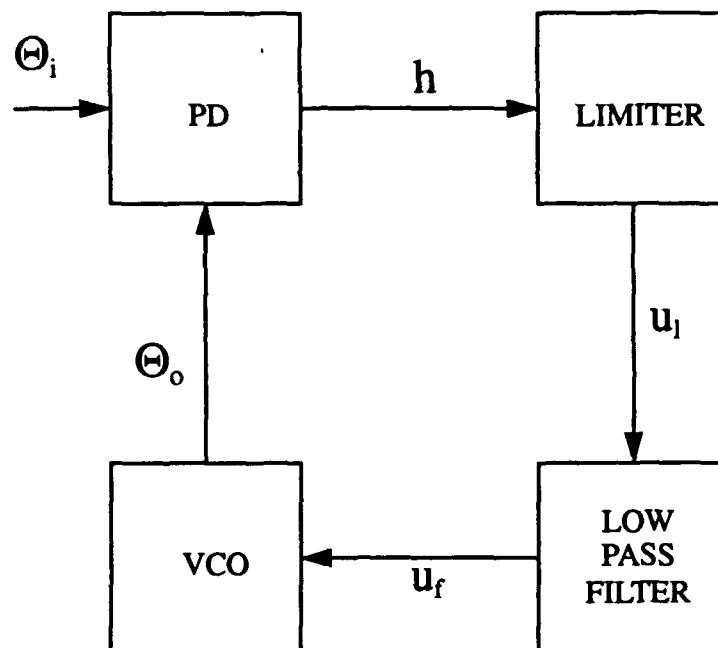


FIGURE 104. Analogue Phase Lock Loop

The phase detector is taken as an ideal multiplier, so if the wave form of the inputs is sinusoidal the waveform of the output is also sinusoidal, and if the inputs are square waves the output is a symmetrical triangle wave.

3.8.3 Mathematical Models

Different Mathematical models were used to represent the system depending on the form of the input. It was possible however, to derive a differential equation which provided a general description of the system.

The output of the filter can be written

$$u_f = f \times u_l \quad (64)$$

where f is the response function of the filter and the \times indicates convolution. It is assumed that the above equation is applied only for the time that the limiter remains in a given state; i.e. when the output of the limiter is a constant. This constant, which shall be designated by a , is either $+1$ or -1 depending on the sign of h . Each time the limiter switches states, we note the values of all relevant parameters, and use these as the initial conditions

for solving eq(64) or its equivalent for the next period that the limiter remains in the same state. Eq(64) is equivalent to

$$\frac{du_f}{dt} + u_f \tau_1 = a \quad (65)$$

The term involving τ_2 vanishes because of the constant limiter output. Substituting for u_f from eq(63) and then substituting for the phase of the VCO output from eq(61) results in a second order differential equation in the phase difference Φ . Rewriting this equation in the standard form of two coupled first order equations we have

$$\frac{d\Phi}{dt} = g \quad (66)$$

$$\frac{dg}{dt} + \frac{g}{\tau_1} = \frac{d^2\Theta_i}{dt^2} + \left[\frac{1}{\tau_1} \right] \frac{d\Theta_i}{dt} - (\omega_o + aK) \left[\frac{1}{\tau_1} \right] \quad (67)$$

3.8.4 Frequency Modulation

For the case of FM, the inputs to the phase detector are sinusoids and so the output of the phase detector is a sinusoid. For FM Θ_i is given as follows

$$\frac{d\Theta_i}{dt} = \omega_i + M \sin(\omega_m t) \quad (68)$$

where ω_i is the carrier frequency of the incoming signal, ω_m is the modulation frequency and M is the modulation index. Taking the second derivative and substituting into eq(67) we get

$$\frac{dg}{dt} + \frac{g}{\tau_1} = [M \sin(\omega_m t) + (\delta\omega - aK)] \left[\frac{1}{\tau_1} \right] + M\omega_m \cos(\omega_m t) \quad (69)$$

Where

$$\delta\omega = \omega_i - \omega_o$$

Integrating eq(69) we get

$$g = M \sin(\omega_m t) + (\delta\omega - aK) + C_1 e^{-\frac{t}{\tau_1}} \quad (70)$$

where C_1 is a constant of integration. Substituting for g in eq(66) and integrating we obtain the following equation for Φ .

$$\Phi = -\frac{M}{\omega_m} \cos(\omega_m t) + (\delta\omega - Ka)t - C_1 e^{-\frac{t}{\tau_1}} + C_2 \quad (71)$$

where C_2 is a constant of integration. The two constants of integration are determined when the limiter switches. At the point at which input voltage to the limiter (h) switches sign the time, phase difference, and derivative of the phase difference (g) are noted and then the integration constants for the next period that h keeps the same sign are determined from these quantities. The form of h is

$$h = \cos(\Phi)$$

the term proportional to the sum term of the input phases

$$\Theta_i + \Theta_o$$

is ignored since the low pass filter rejects these high frequencies. Thus the a in the above equations is determined by the cosine of the phase difference.

3.8.5 BPSK

For BPSK the input phase is of the form

$$\Theta_i = \omega_i t + \chi$$

where χ is the phase constant which takes on the values of either 0 or π . For the purpose of simulating the behavior of the system the value of χ is selected randomly every signaling period. The voltage in to the phase detector is of the form

$$[\cos\Theta_i]^2$$

Thus the output of the phase detector h is given as

$$h = \frac{1}{4} [2\cos(\Theta - \Phi) + \cos(\Theta + \Phi)] \quad (72)$$

where Φ is the phase difference as before, and the terms involving the sum of the input phase and the output phase of the VCO have been discarded because these frequencies would be rejected by the low pass filter.

If we now substitute in eq(67) for Θ_i we obtain the following differential equations for the phase difference and its derivative:

$$\frac{d\Phi}{dt} = g \quad (73)$$

$$\frac{dg}{dt} + \frac{1}{\tau_1} g = \frac{1}{\tau_1} (\omega_i - \omega_o - aK) \quad (74)$$

where the symbols have the same meaning as they did in the FM case; $a = +1$ if $h > 0$ and $a = -1$ if $h \leq 0$. As before we integrate during a period when the output of the limiter is constant. (The times when the output of the limiter changes depend in part on the signaling rate.)

The solution to the above equations is

$$\Phi = c + (\omega_i - \omega_o - aK) (t - \tau_1) + b \exp((t_0 - t)/\tau_1) \quad (75)$$

$$g = (\omega_i - \omega_o - aK) + \left[-\frac{b}{\tau_1} \right] \exp((t_0 - t)/\tau_1) \quad (76)$$

where t_0 is the time when the limiter switched sign and the constants c and b are determined from the values of the phase and its derivative at the time the switch occurs.

3.8.6 Square Waves

Tetsuro and Chua found that a second order phase lock loop (without a limiter) with square waves as input behaved differently than sinusoids and gave chaotic behavior.³ The presence of the hard limiter modifies the behavior of the system so that it is the same for square waves and for sinusoids. This happens because if the inputs to an ideal multiplier are square waves the output is a symmetric

triangular wave. As can be seen from FIGURE 105 a symmetric triangular wave and a sine wave are positive and negative for the same periods of time (assuming of course that they have the same period). Since the limiter responds only to the sign of the wave form input to it and not the shape the square waves will behave the same way a sine does.

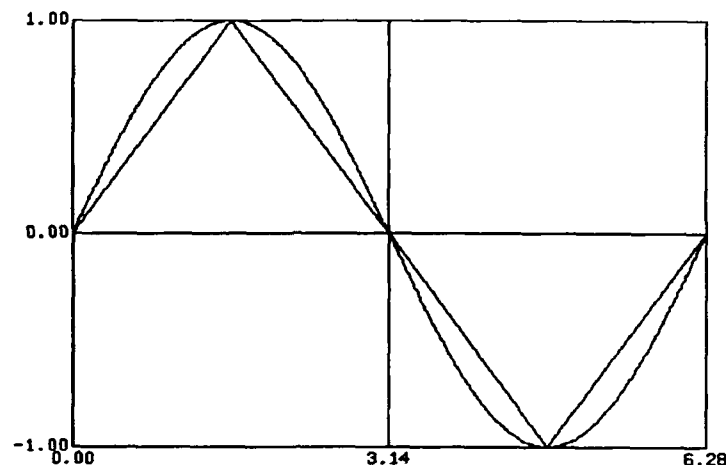


FIGURE 105 Comparison of sine and triangle waves

3.8.7 Numerical Simulations

In order to study the behavior of the PLL for the different waveforms, computer programs were written in C which ran on a SUN SPARC station 1 under UNIX. Each of the waveforms studied required its own set of programs. However, the programs were very similar, (the major difference between them being the criteria for the limiter switching states) and so will be described together.

The first step in the study was to determine when the limiter switched states. This was done in a computer program which found when the function h , described in paragraphs 1.2.1 and 1.2.2, went to zero. The computer program used an algorithm based on a simple enclosure method⁴. The inputs to this program were the values of the filter parameters, the difference between the VCO free running frequency and carrier frequency of the incoming wave, the gain of the VCO, the initial values of the phase difference and its derivative, the initial time, and the total time over which the system was to run. The program for the FM simulation also required the modulation index and the modulation frequency. The BPSK simulation required the signalling period, and contained a pseudo random number generator from the C library. The outputs of the zero finding program, were the phases, derivatives of the phases and the times when the limiter switched states; the BPSK program output also contained the values of the phase constant at the time of the limiters switching states.

The next step was to find the values of the phase, and the time derivative of the phase at sample times between the switching times of the limiter. (The so called trajectories of the

system.) This program solved the equations for the phase and its derivative given in paragraphs 3.8.4 and 3.8.5. The inputs to the program were the same as the inputs to the zero crossing programs, the outputs from that program, and the time interval between the sample points. The outputs were the sample times, phase and the derivative of the phase at the sample times. The output files were such that phase space diagrams and configuration space diagrams could be generated from them.

A specialized form of the above program was used to generate surfaces of section⁵. Here the sampling time interval was fixed by the inverse of the frequency in the FM case, and by the inverse of the signalling rate in the BPSK case.

It was found that, just as in the linearized analysis of PLL, one of the crucial parameters governing the behavior of the PLL was the ratio of the VCO amplification K to the difference $\omega_i - \omega_o (\equiv \delta\omega)$. A program was written which calculated the surfaces of section and recorded them in a file as functions of this ratio. The file was then used to create a bifurcation plot.

One of the traits of a non-linear system which provides an indication of whether the system is in a chaotic mode, is the power spectrum of the system³. A program was written which calculated the power spectrum of a time series. The inputs were phase and time as gotten from the previously mentioned programs, and the output was the amplitude of the phase squared at discrete frequencies.

Finally two programs were written to calculate the Liapunov exponentials^{5,6} for two trajectories of the system which began with slightly different initial conditions. The first program calculated the distances between the two trajectories and then did a least squares fit to an exponential, the second calculated the exponential directly using a renormalizing algorithm suggested in reference 5. The programs took as input the phase versus time outputs of the trajectory programs and gave as output the Liapunov exponent. The second program gave a time sequence of the exponential so that it was possible to see whether a "steady state" had been reached.

The next paragraph describes some of the results from the use of these programs.

3.8.8 Results and Conclusions

This subsection is divided into two parts. The first part presents some of the results for FM and conclusions based on these results. The second part presents some of the results for BPSK. The investigation of BPSK is not yet concluded.

FM

In all of the figures discussed in this section the initial time and phase derivative were set equal to zero and the initial phase was set equal to 1. The filter constant τ_1 was taken as 0.01 seconds, the modulation index as 10 and the frequency of modulation as 1000 Hz. These values were selected, after many runs with different values, as giving characteristic results for the system.

FIGURE 106. is a plot of Φ vs. time for the system with $K/(\delta\omega) = 10$. FIGURE 107. is a phase plot for the same value of the ratio.

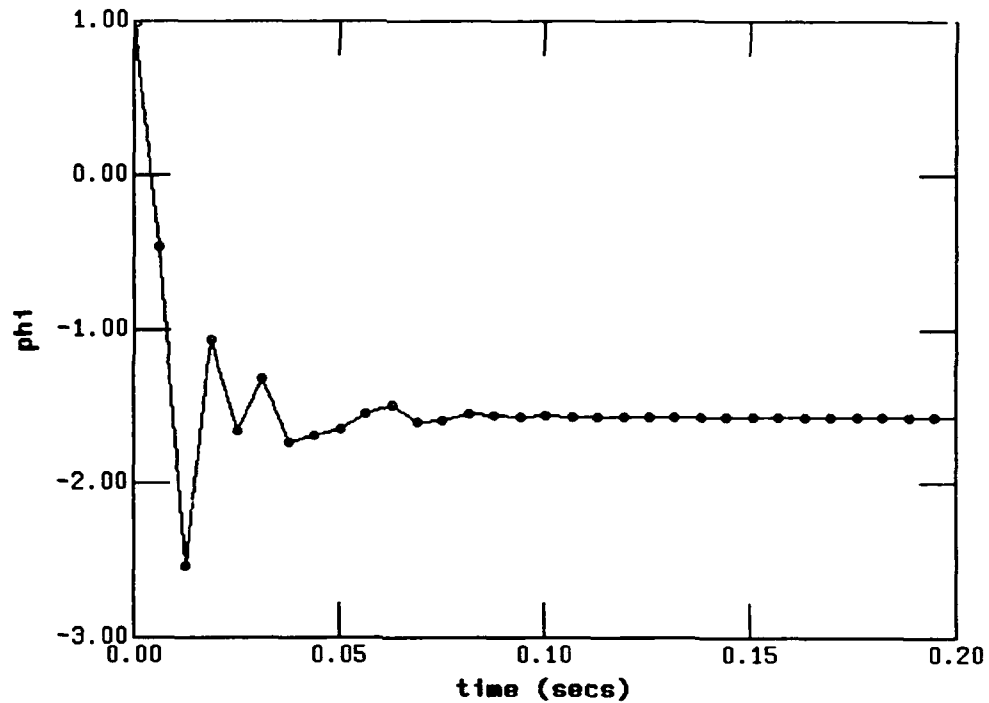


FIGURE 106. Phi vs. time for FM with $K/(\delta\omega) = 10$

FIGURE 106. shows that the phase rapidly converges to an equilibrium value. The phase plot has the appearance of an ω limit cycle⁷ suggesting that the system settles into a stable, non-chaotic mode of operation. This result is in agreement with the usual linear analysis of PLLs. Further confirmation of this behavior is provided by the power spectrum (FIGURE 108) and the surface of section (FIGURE 109.). Finally the leading Liapunov exponent for $K/(\delta\omega) = 10$ is < 0 indicating stable, non-chaotic behavior.

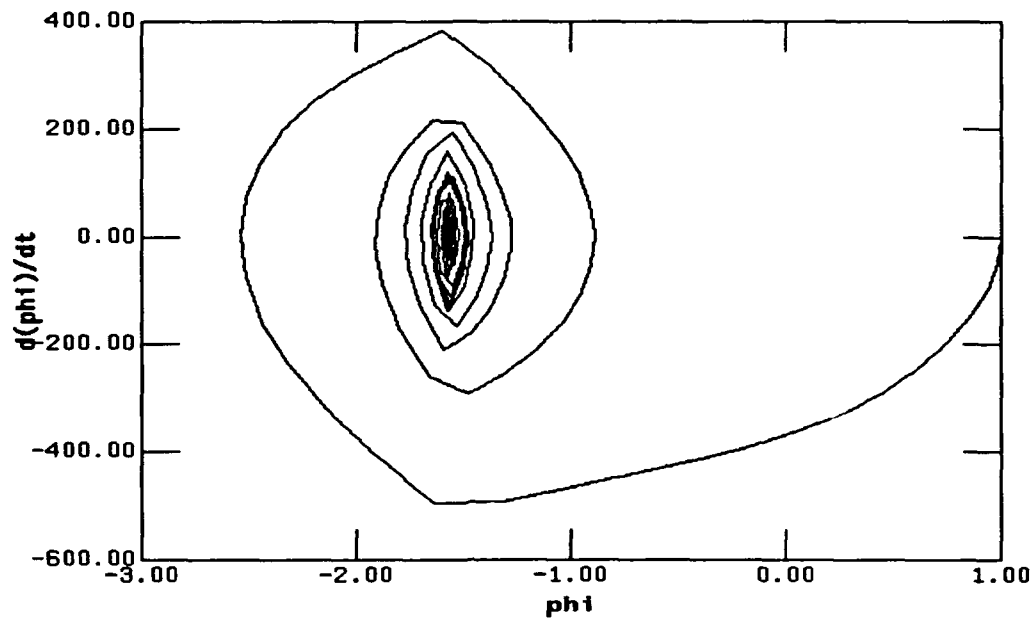


FIGURE 107. Phase space plot for FM with $K/\delta\omega = 10$

FIGURE 110. is a bifurcation diagram of the equilibrium values of ϕ , as calculated from a surface of section, as a function of the ratio $K/(\delta\omega)$. The upper diagram is a magnified version of the lower diagram. Note the differences in the values on the axis. From the diagram it can be seen that the equilibrium phase goes from having many values to fewer and fewer values as the ratio increases. The structure of the diagram is complex for values of the ratio between 1 and 2. There are many more equilibrium values between $K/(\delta\omega) = 1$ and 1.3, then for values between 1.3 and 1.4 the structure seems to simplify, become more complicated between 1.4 and 1.5, settle into two values between 1.5 and 1.7 then go to one value then back to two about 1.78 and back to 1 for ratios greater than about 1.82. So it would seem that the system goes from being complex (possibly chaotic) for low values of the ratio and that stabilizes into a non chaotic mode for ratios greater than 1.82.

To see if the behavior of the system is "chaotic" for values of the ratio less than 1.3, the behavior was examined for the ratio equal to 1.24. FIGURE 111. is a plot of the phase vs. time for this ratio and FIGURE 112. is phase space plot for the same ratio.

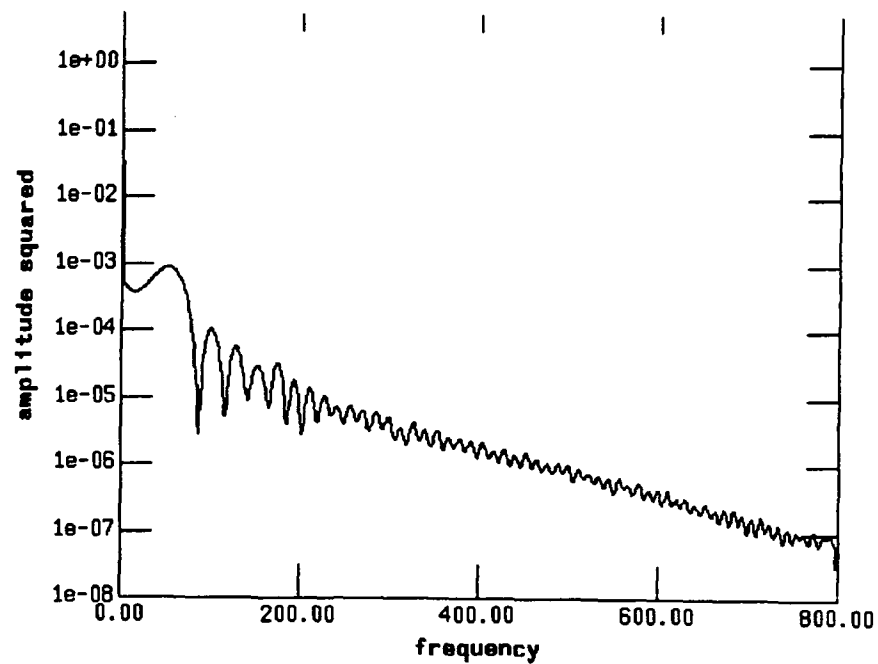


FIGURE 108 Power Spectrum for FM with $K/\delta\omega = 10$

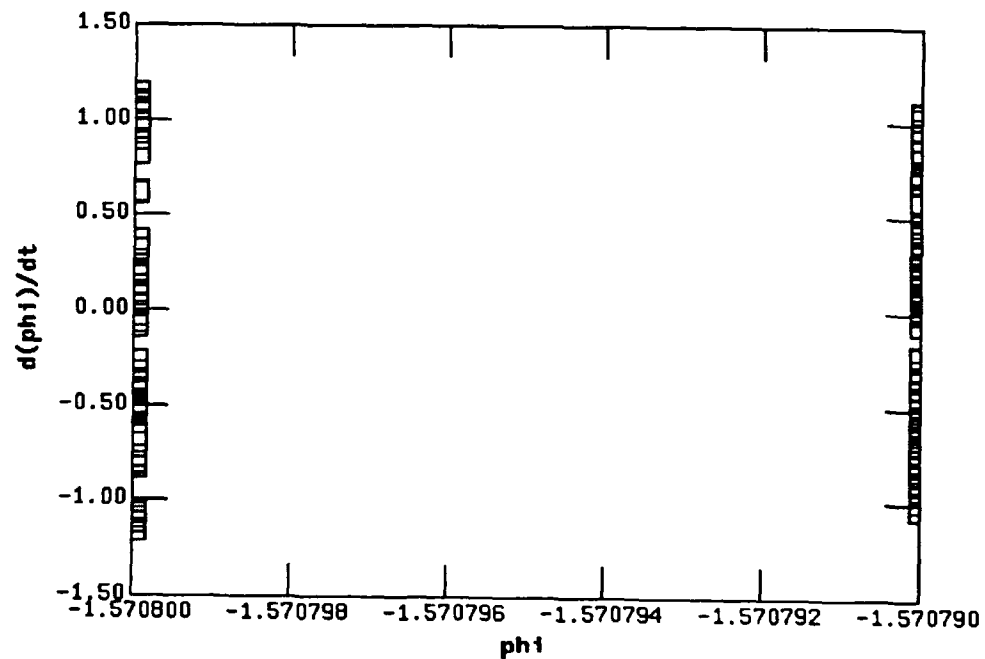


FIGURE 109. Surface of section for FM with $K/(\delta\omega) = 10$

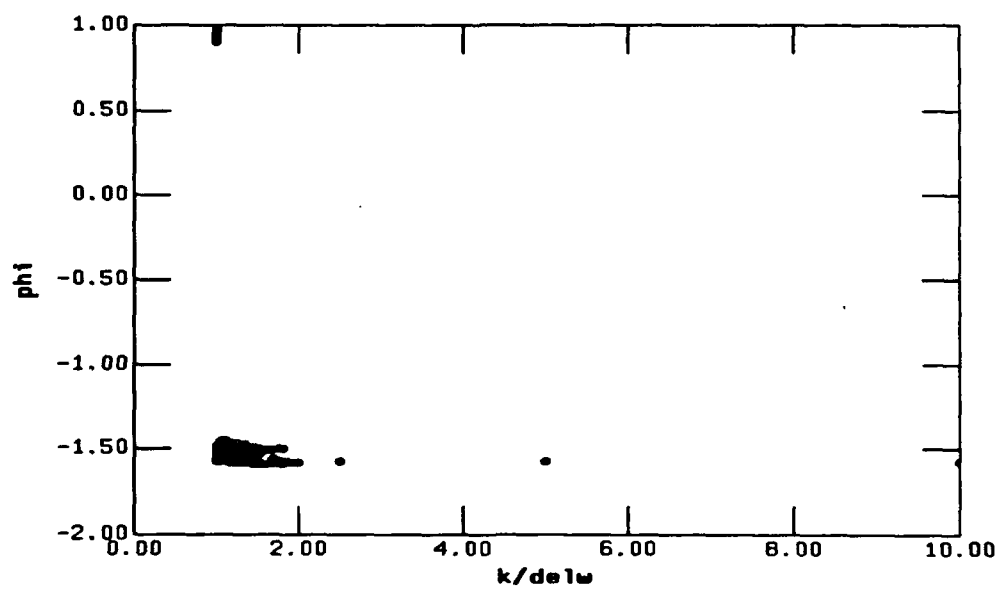
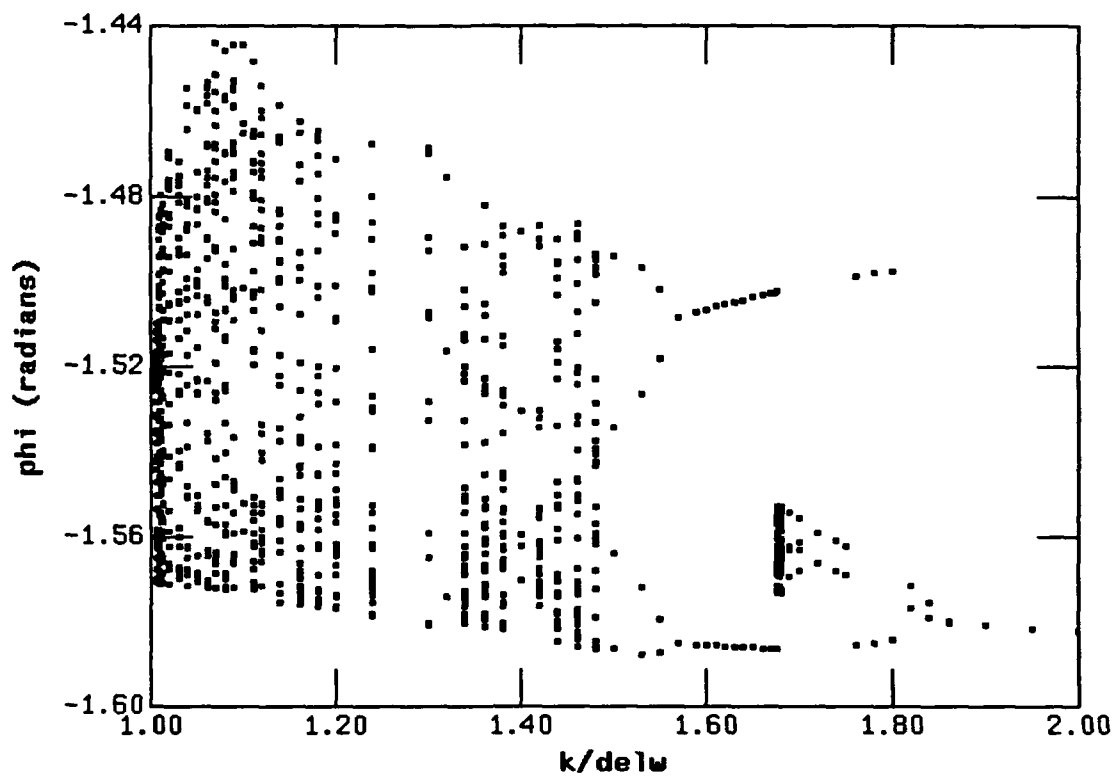


FIGURE 110. Bifurcation diagram for FM

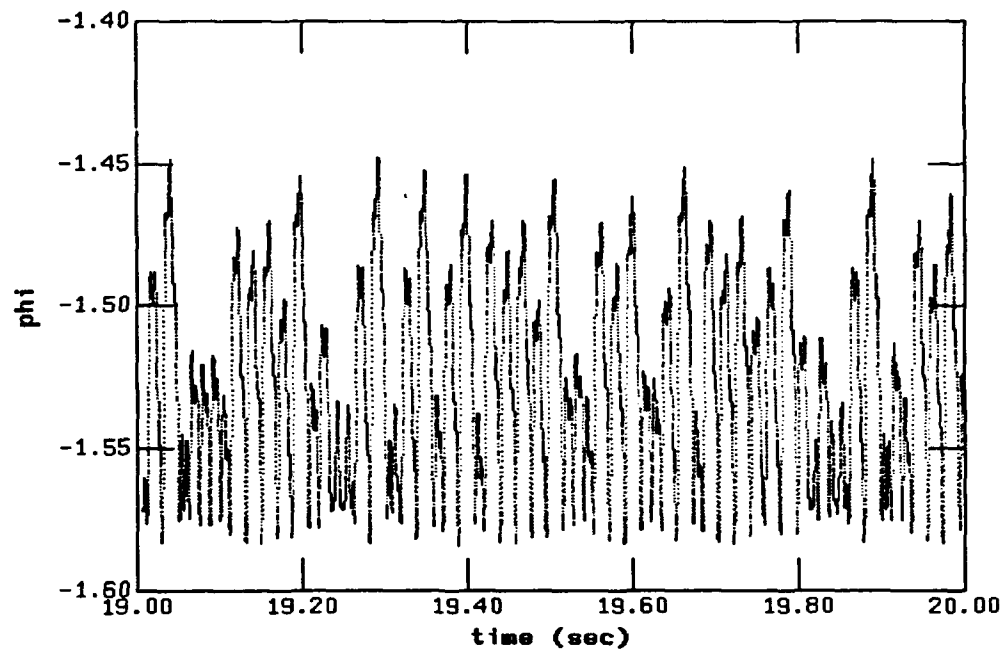


FIGURE 111. Phi vs. time for FM with $K/(\delta\omega) = 1.24$

Comparing them to the plots for $K/(\delta\omega)=10$ we see that they are much more complex. There does not appear to be a limit cycle in the phase plot though there appears to be a many period set of limit cycles. The power spectrum (FIGURE 113) and the surface of section (FIGURE 114.) also appear quite complex- indicating possible chaos. A calculation of the leading Liapunov exponent gives a number greater than zero. Thus all the indications are that the behavior of the system for $K/(\delta\omega)= 1.24$ is chaotic. Since this choice of the ratio was representative of the values of the ratio between 1 and 1.3 we can conclude that the system behaves chaotically in this range.

The study of the PLL with an FM input has shown that:

- a) There is a region of chaotic behavior. This region, however, occurs in a range of parameters where the loop is not usually operated.
- b) In the region of parameter values where the PLL is usually operated the behavior is non chaotic and stable. Further the non-linear analysis agrees with the linear analysis.

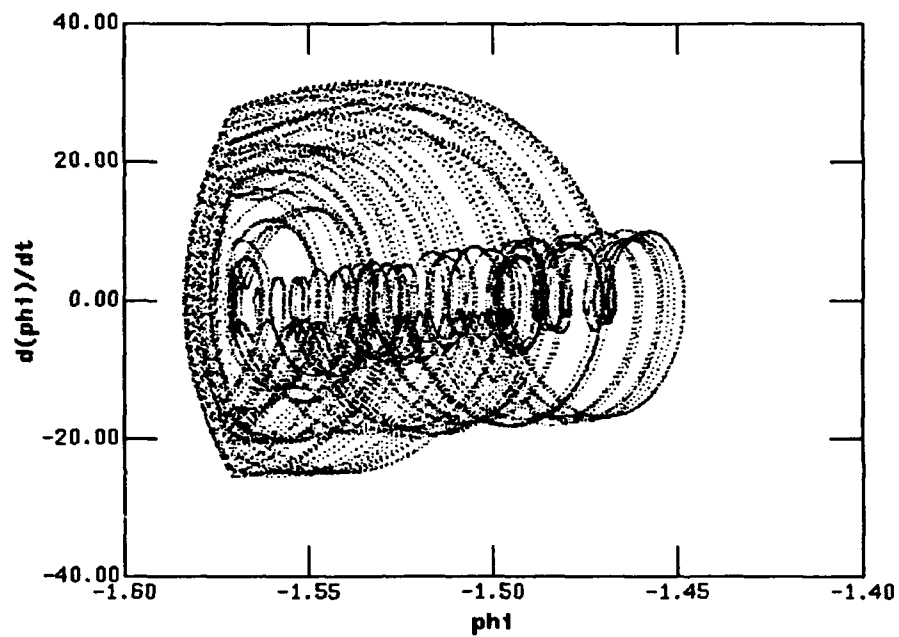


FIGURE 112. Phase Diagram of Fm with $K/(\delta\omega)=1.24$

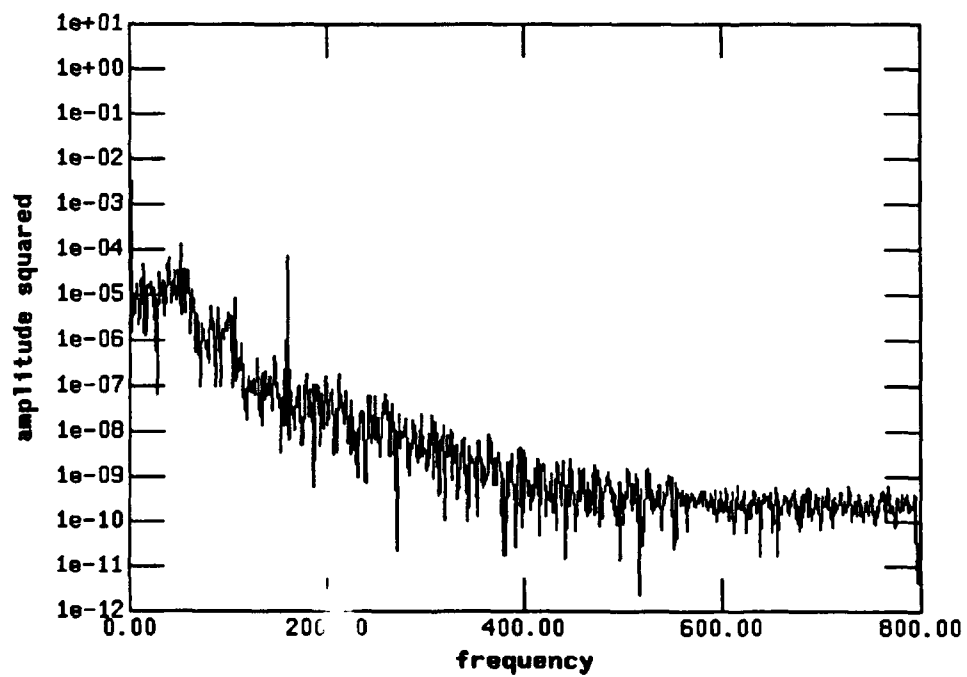


FIGURE 113 Power Spectrum of ϕ for FM with $K/(\delta\omega)=1.24$

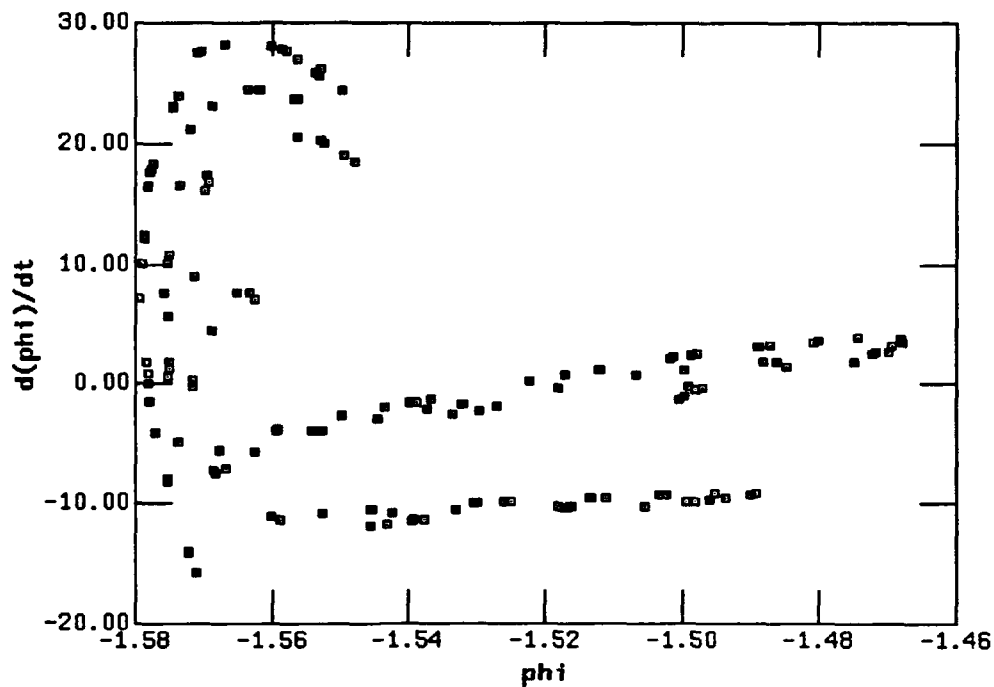


FIGURE 114. Surface of Section for FM with $K/(\delta\omega) = 1.24$

BPSK

The study of the PLL with a BPSK input is not yet complete. The preliminary results are presented here. Again as in the FM case the study was primarily conducted by fixing all the parameters except the ratio $K/(\delta\omega)$. In all of the figures discussed in this section the initial time, the initial phase constant, and initial phase derivative were set equal to zero and the initial phase was set equal to 1. The filter constant τ_1 was taken as 0.01 seconds, signal rate as 100 Hz, and the input carrier frequency as 1000 Hz.

FIGURE 115. is a plot of phase versus time for $K/(\delta\omega) = 10$. As can be seen from the figure the phase is increasing linearly and does not seem to be approaching an equilibrium value. This was true for all values of $K/(\delta\omega)$ studied. The phase plot in FIGURE 116. is a "polar plot". It is quite lovely and quite complex. Further work needs to be done in order to understand how to interpret it. The power spectrum in FIGURE 117. shows no features indicating chaos, nor any discrete frequencies. Finally the bifurcation diagram in FIGURE 118. shows more and more complex structure as the ratio of $K/(\delta\omega)$ increases. Calculations of the leading Liapunov exponent were inconclusive.

Because of the rich phase diagram there would seem to be interesting structures to be investigated in the case of a PLL with a BPSK input. A part of the effort for the next year will be devoted to this investigation

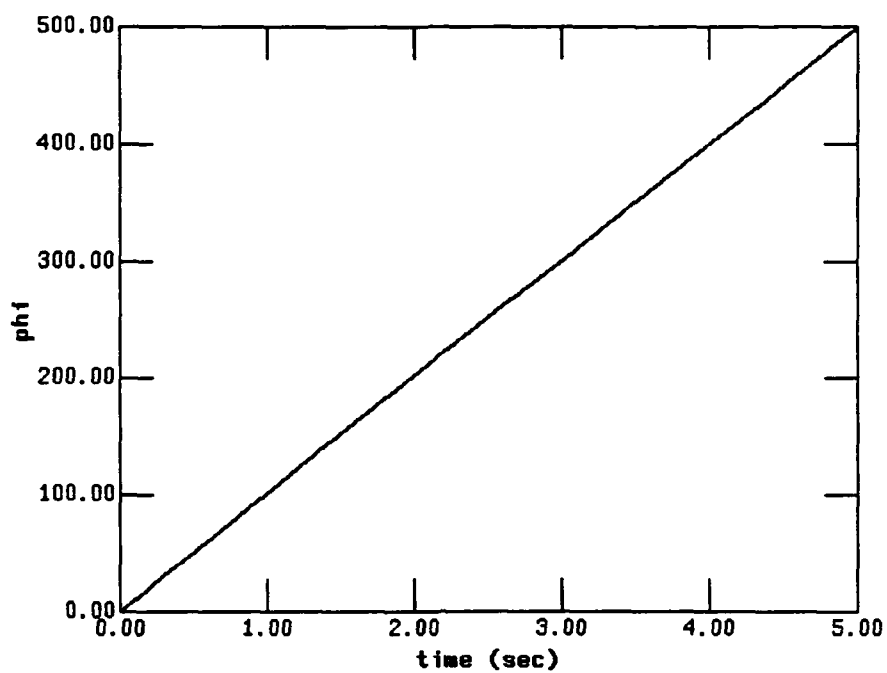


FIGURE 115. Phi vs. time for BPSK with $K/(\delta\omega) = 10$

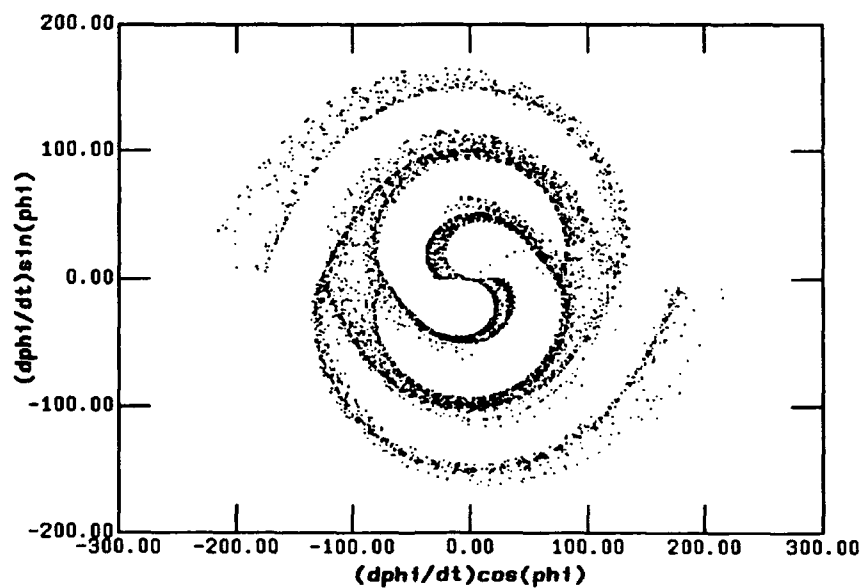


FIGURE 116. Phase plot for BPSK with $K/(\delta\omega) = 10$

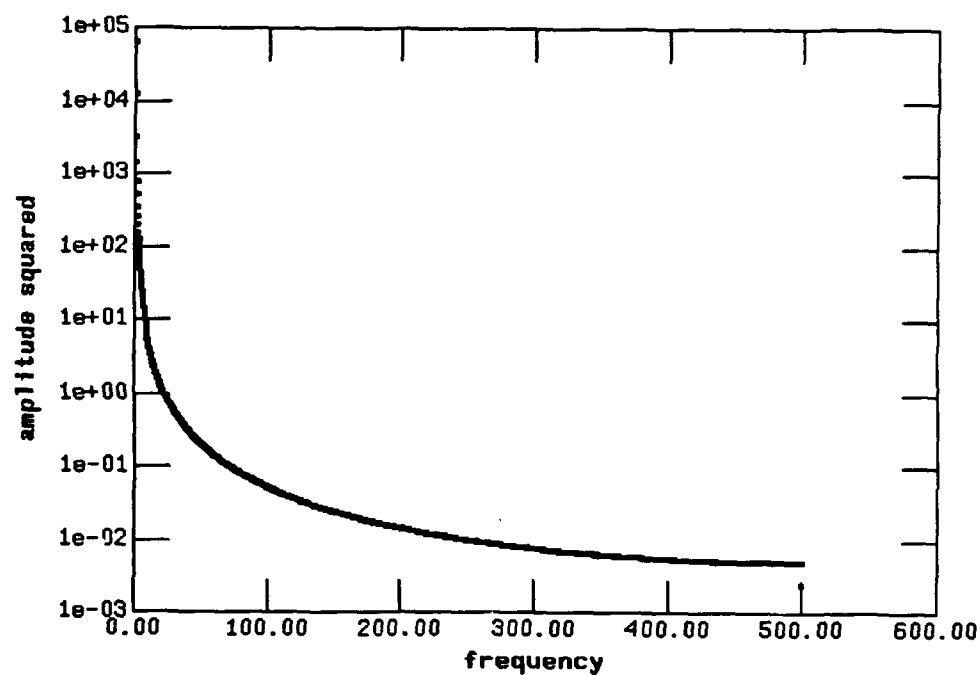


FIGURE 117. Power Spectrum for BPSK with $K/(\delta\omega) = 10$

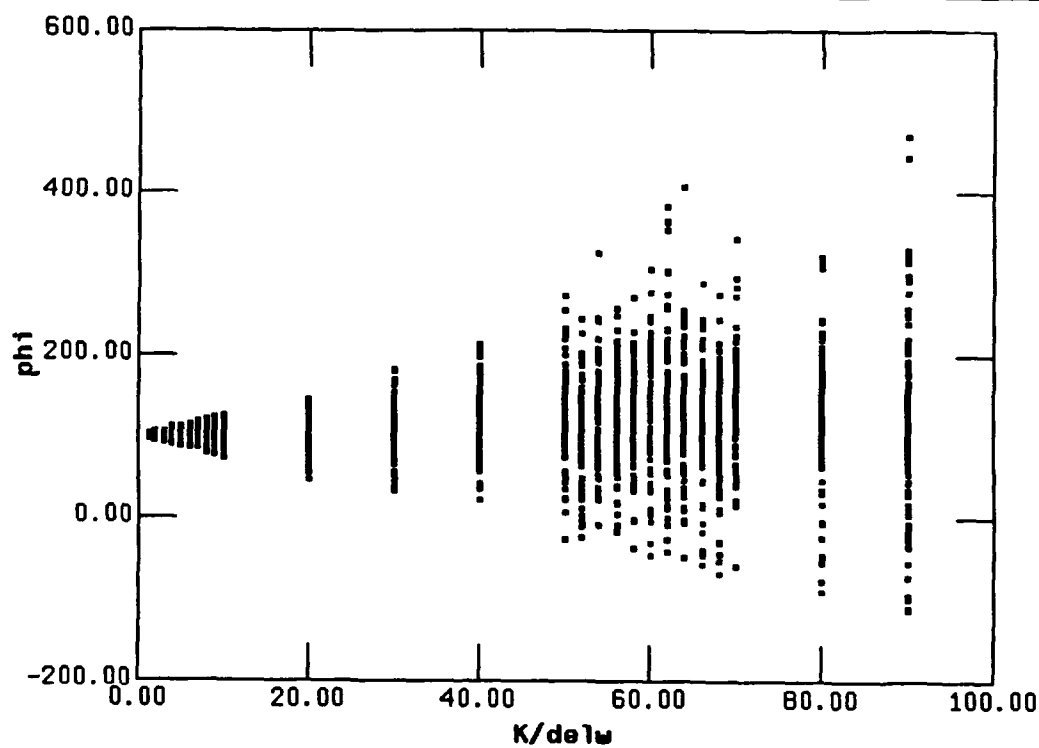


FIGURE 118. Bifurcation diagram for BPSK

3.8.9 References

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3.9 Synchronization of Digital Coupled Oscillators

3.9.1 INTRODUCTION

Coupled oscillators are common in many scientific areas, including communications, optics, engineering, chemical reactions, biology, etc. This type of system has attracted much attention (see, for example, references 1-4 and references therein), beginning with Winfree⁵ who discovered that a class of coupled oscillators with different internal frequencies suddenly synchronize to a common frequency when the coupling between oscillators exceeds a critical value. Winfree and others suggested that these models could give insight into the behavior of coupled biological rhythms, such as swarms of fireflies that flash in synchrony, synchronous firing of cardiac pacemaker cells, groups of women whose menstrual cycles become synchronized, etc.⁵

The synchronization of oscillators has important practical applications in electronic systems. For example, in the design of microwave systems the power of many devices may be combined through synchronization to achieve power that increases quadratically with the number of oscillators. In this case the oscillators must have not only the same frequency, but should also be in phase. Similar needs are found in electrical power generation, Josephson junction arrays, etc. Another important application of synchronization is related to a network of clocks distributed geographically in different locations, where it is necessary to have the same time for all clocks. For this type of application, electronic devices such as phase locked loops (PLL) have been studied⁶.

Coupled digital phase locked loops (DPLL's) can also be used as a synchronizing device in a network of elements. Gil and Gupta⁷ showed that a single first order DPLL is governed by a nonlinear difference equation, which displays regular and chaotic behavior. We have observed similar features in two or more coupled DPLL's and the boundaries between synchronized and chaotic behavior have been determined⁸.

In this section we study networks of coupled DPLL's with and without variability in their component elements. Our attention is concentrated on three types of geometries, namely, ring, double ring and global coupling. The paper is organized as follows: In section 3.9.2 we briefly review the basic properties of a digital phase locked loop, and of two coupled DPLL's. In section 3.9.3 we develop the formalism for many interconnected devices in the three configurations mentioned above. Section 3.9.4 gives the conclusions and discussions of the problems considered.

3.9.2 ONE AND TWO LOOPS

A single, first order, digital phase locked loop consists of a sample and hold (SH) and a variable frequency oscillator (VFO) as shown in FIGURE 119. The VFO runs with an internal frequency Ω in the absence of an input signal. Its output is given by $v(t)=A \sin \omega t$, where ω is its instantaneous frequency. When $v(t)=0$ with a positive slope, the VFO sends a signal to the SH and a sample $v(t_k)$ is taken from the input signal. The frequency of the VFO at this instant is adjusted according to

$$\omega' = \Omega + bv(t_k) \quad (77)$$

As a consequence there is possibility of locked behavior when the VFO samples at a constant phase value. The dynamical behavior of a single DPLL, governed by eq(77), was studied in detail in⁹. It was shown that when the input signal of a single loop is a sinusoid, then the time evolution of the phase difference between input signal and the VFO output is described by a circle map. This type of map has been studied extensively in the past¹⁰. It exhibits periodic, quasiperiodic and chaotic behavior.

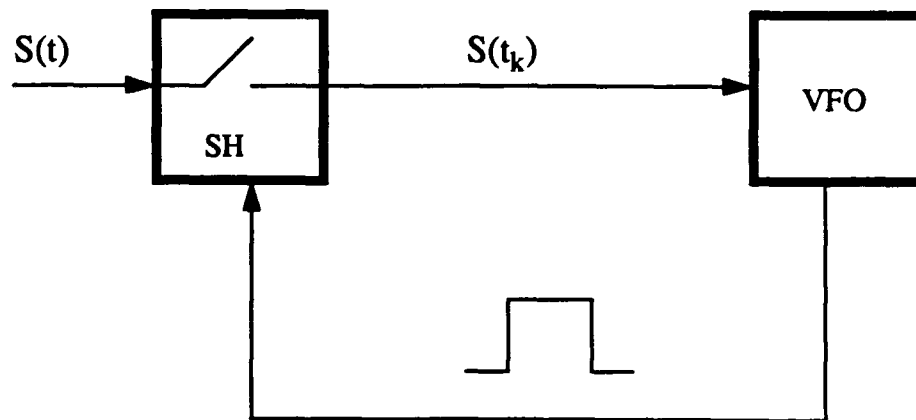


FIGURE 119. Schematic representation of a single first order phase locked loop

We will be concerned in this paper with coupled DPLL's, where the input of a loop is given by a combination of the outputs of the other loops. Each loop i has its own set of parameters Ω_i and b_i . We start by analyzing two coupled DPLL's where the input to one loop is the output of the other loop, and vice-versa. This system was described in sections 3.1 and 3.2. Here we review some of the main features and report some different results for the coupled loops. A schematic representation of

the system is shown in FIGURE 120. In the dynamical evolution, every time that one of the VFO signals crosses zero with a positive slope this oscillator sends a signal to its SH and a sample is taken from the output of the other loop. The loop that samples switches its frequency to a new value determined by eq(77).

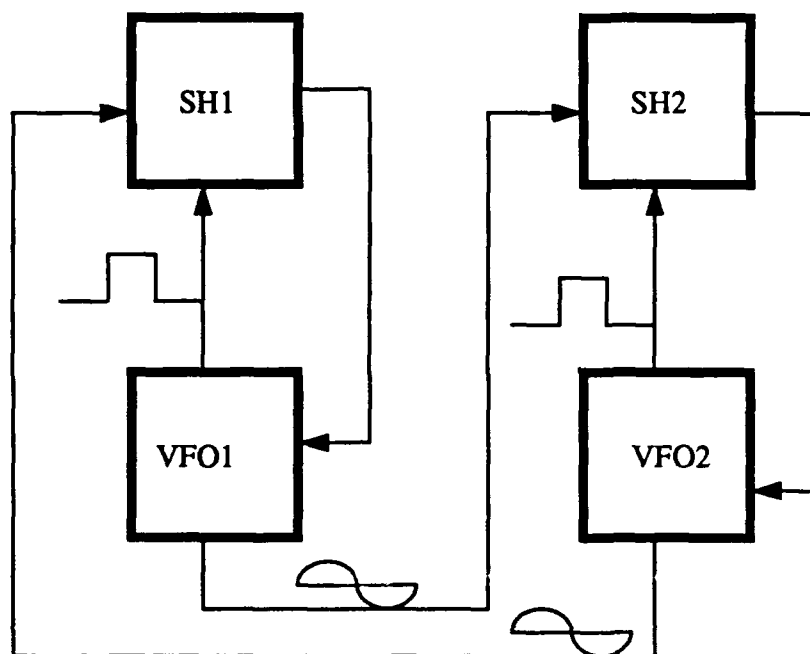


FIGURE 120. Schematic representation of two self synchronized DPLLs

The equations that govern the dynamics of the loops are

$$\omega'_1 = \Omega_1 + b_1 A_2 \sin \phi_2, \phi_1 = 0 \quad (78a)$$

$$\omega'_2 = \Omega_2 + b_2 A_1 \sin \phi_1, \phi_2 = 0 \quad (78b)$$

The gain b_i of the VFO appears always multiplied by the amplitude A_j ($j \neq i$) of the input signal. Thus without loss of generality we can take $A_i = 1$. Also, dividing both equations by one of the center frequencies, say Ω_2 , the parameters and variables become dimensionless. We keep the same notation and simply take $\Omega_2 = 1$, having in mind that now we are working with renormalized dimensionless quantities. In this way, we have

$$\omega'_1 = \Omega_1 + b_1 \sin \phi_2, \phi_1 = 0 \quad (79a)$$

$$\omega'_2 = 1 + b_2 \sin \phi_1, \phi_2 = 0 \quad (79b)$$

We consider that the gains are positively defined. Since the frequencies of these time discrete systems are also positive we must have $b_1 \leq \Omega_1$ and $b_2 \leq 1$.

When the loops synchronize to a common frequency ω_s we have $\omega_1 = \omega_2 \equiv \omega_s$ and $\phi_2(\phi_1 = 0) = -\phi_1(\phi_2 = 0) \equiv \Delta\phi$. Putting this into eq(79a) and eq(79b), we obtain

$$\omega_s = \frac{\Omega_1/b_1 + 1/b_2}{1/b_1 + 1/b_2} \quad (80)$$

and

$$\sin\Delta\phi = \frac{|\Omega_1 - 1|}{b_1 + b_2} \quad (81)$$

From eq(81) one sees that the synchronization is possible only if

$$b_1 + b_2 \geq |\Omega_1 - 1| \quad (82)$$

If $b_1 + b_2$ is smaller than the critical value determined by eq(82), then the synchronization does not occur, and quasiperiodic behavior is observed.

We show in FIGURE 121. the bifurcation diagram for a coupled loop system where $b \equiv b_1 = b_2$ and $\Omega_1 = 1.2$. The quantity plotted is ω_1 vs. b . As b increases we observe a quasiperiodic regime, which ends at the point determined by eq(82), which is followed by a synchronized regime, bifurcations, and chaos. In our numerical calculations we evolve the system according to the algorithm given in reference 9.

In reference 8 we investigated the system where the center frequencies of both loops were identical, i.e., $\Omega_1 = \Omega_2 \equiv \Omega$. In that case, from eq(80) and eq(81) we obtain that in the synchronized state $\omega_s = \Omega$ and $\Delta\phi = 0$. Through a linear stability analysis we showed that this state is stable for $0 < b_1 + b_2 < \Omega/\pi$. When the couplings, i.e., the gains, increase beyond this value the system passes through a sequence of period doubling bifurcations, governed by Feigenbaum's¹¹ exponents, followed by a chaotic regime

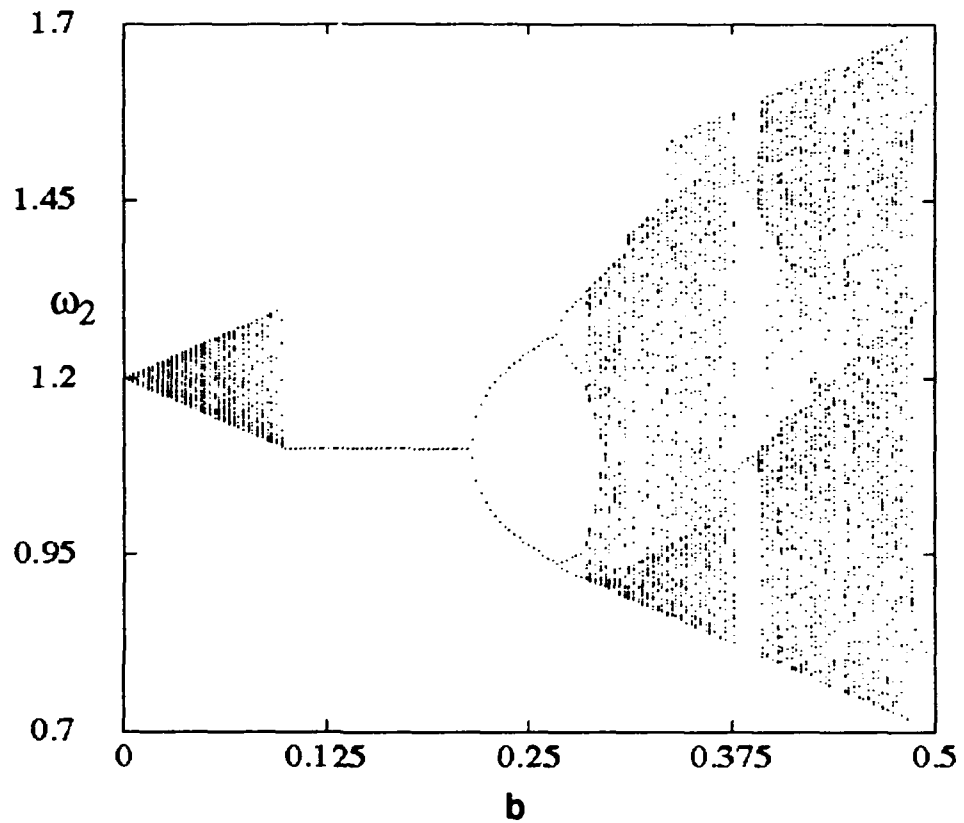


FIGURE 121. Frequency of loop1 vs. $b \equiv b_1 = b_2$ for $\Omega_1 = 1.2$

3.9.3 MANY COUPLED OSCILLATORS

We now turn our attention to populations of many coupled oscillators. In such a system, every time that a VFO signal crosses zero with a positive slope the SH in that loop takes a sample from combined outputs of the other VFO's to which it is connected. The input to the i th sampler is assumed to be given by a linear combination of the VFO outputs of the other loops, that is,

$$s(t_i) = \sum_{j=1}^N a_{ij} v(\phi_j(t_i)) \quad (83)$$

The matrix $A=[a_{ij}]$ is called the interconnection matrix for the system. If loop i receives input from loop j then $a_{ij} = 1$. Otherwise $a_{ij} = 0$. We consider $a_{ii} = 0$.

The value $s(t_i)$ is used to adjust the frequency of the i th VFO according to

$$\omega'_i = \Omega_i + (b_i/n_i) s(t_i) \quad (84)$$

where

$$n_i = \sum_{j=1}^N a_{ij}$$

is the number of loops from which loop i receives input. In the synchronized state all the loops run with the same frequency $\omega'_i = \omega_s$. From eq(83) and eq(84) we obtain

$$\omega_s = \Omega_i + \frac{b_i}{n_i} \sum_j a_{ij} \sin(\phi_j), \phi_i = 0 \quad (85)$$

Using eq(85) and summing over all the loops, we have

$$\sum_i \frac{\omega_i - \Omega_i}{b_i/n_i} = \sum_{i,j} a_{ij} \sin(\phi_j), \quad (\phi_i = 0) \quad (86)$$

If between two loops that are connected the communication exists in both directions, i.e, if $a_{ij} = 1$ then $a_{ji} = 1$, then the r.h.s. of eq(86) vanishes. This happens because $\phi_j(\phi_i = 0) = -\phi_i(\phi_j = 0)$ and $\sin(\cdot)$ is an odd function. Thus the synchronization frequency can easily be obtained from (86) as a weighted average of the Ω_i 's,

$$\omega = \frac{\sum_i \frac{\Omega_i n_i}{b_i}}{\sum_i \frac{n_i}{b_i}} \quad (87)$$

This expression for the synchronization frequency remains unchanged if $\sin(\cdot)$ is replaced by any odd periodic function. We now study two kinds of systems:

Oscillators with identical center frequencies

If all the oscillators have the same center frequency $\Omega_i = \Omega$, then from eq(87) one obtains $\omega_s = \Omega$, as expected. As discussed in the previous paragraphs we can make $\Omega = 1$ without loss of generality. Moreover, a solution with all the phase differences being zero satisfies eq(85) for any configuration. These results are independent of the gains (b_i 's) and of the connection numbers (n_i 's).

Our numerical calculations are concentrated on the three basic types of configurations shown in FIGURE 122., that is, (a) ring, (b) double ring, and (c) global coupling. We observe that the oscillators in these geometries synchronize to a common frequency over a range of the parameter space.

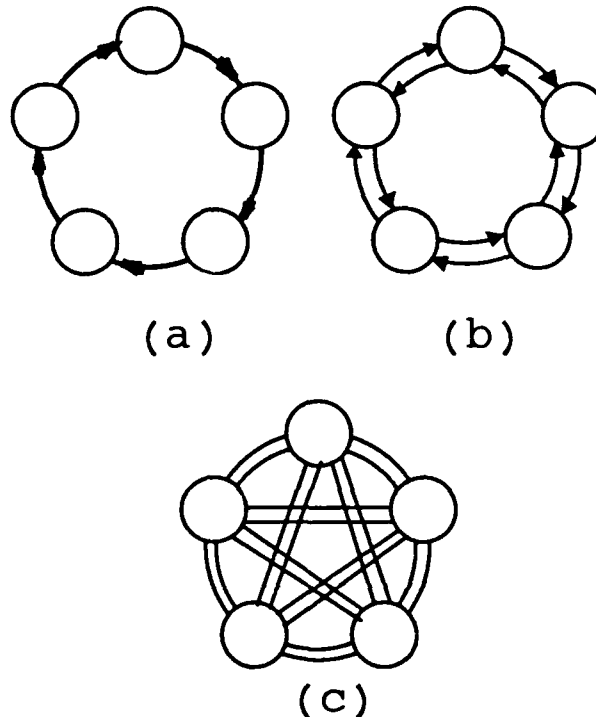


FIGURE 122. Schematic representation for (a) ring, (b) double ring, (c) global coupling configurations for $N = 5$

For the ring configuration the communication between loops is only in one direction. Therefore the derivation for the center frequency performed above is not valid for this system. We observe numerically that the synchronizing frequency for the ring configuration is also Ω , as expected. In this geometry the sum on the r.h.s. of eq(85) has only one term. From that, one can derive immediately that the phase differences between oscillators will be zero. In the double ring and global coupling configurations, the communication between loops is in two directions, which satisfies the conditions for the derivation of eq(87). In these two cases, we also find that the synchronization frequency is Ω and there is no phase difference between loops.

Although the attractor for the synchronized state is the same for all the configurations, the transient behavior strongly depends on the geometry of the system. To study the transient

to the locked state we initiate the system with all loops having the same instantaneous frequency, which is taken to be equal to Ω . We choose the initial phases to be zero, with the exception of the phase of one of the loops, say loop 1. We take the initial phase of this loop to be given by a random number between 0 and 1. We calculate the number of sampling times n of loop 1 that brings the system to the final attractor with a given accuracy ϵ , that is, when $|\Omega' - \Omega_s| \leq \epsilon$. We did simulations for 200 different initial conditions for the phase of loop 1, and calculated the average number of sampling times \bar{n} of loop 1 that brings the system to the final attractor. The gains of the loops were fixed to $b_i = 0.1$. The results are displayed in FIGURE 123. a for a system of 10 loops. The transient is the longest for the ring configuration and the shortest for the global coupling.

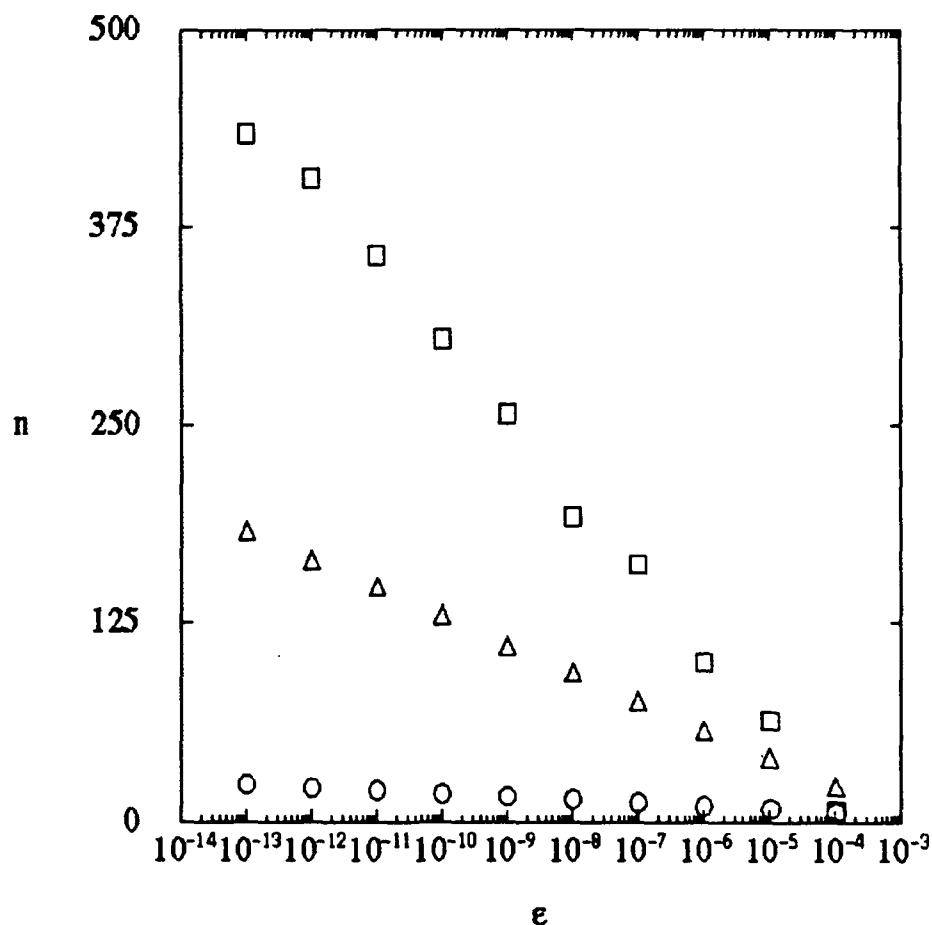


FIGURE 123. a Average number of iterations for the transient that take sloop1 to the final attractor for ring (square), double ring (triangle) and global coupling (circle) for $b = .1$ vs. ϵ for $N=10$

Moreover, \bar{n} is well approximated by the equation

$$\bar{n} = A \log \epsilon + B \quad (88)$$

eq(88) fails in the limit $\epsilon \rightarrow 1$. We also study the transient as a function of the size of the system. We find that, for a given configuration, the average number \bar{n} of iterations per loop for the transient is approximately constant for N sufficiently large. Thus, the total number of samplings increases linearly with the size of the system. The results of \bar{n} vs. N for the double ring, and global coupling configurations are shown in FIGURE 123. b.

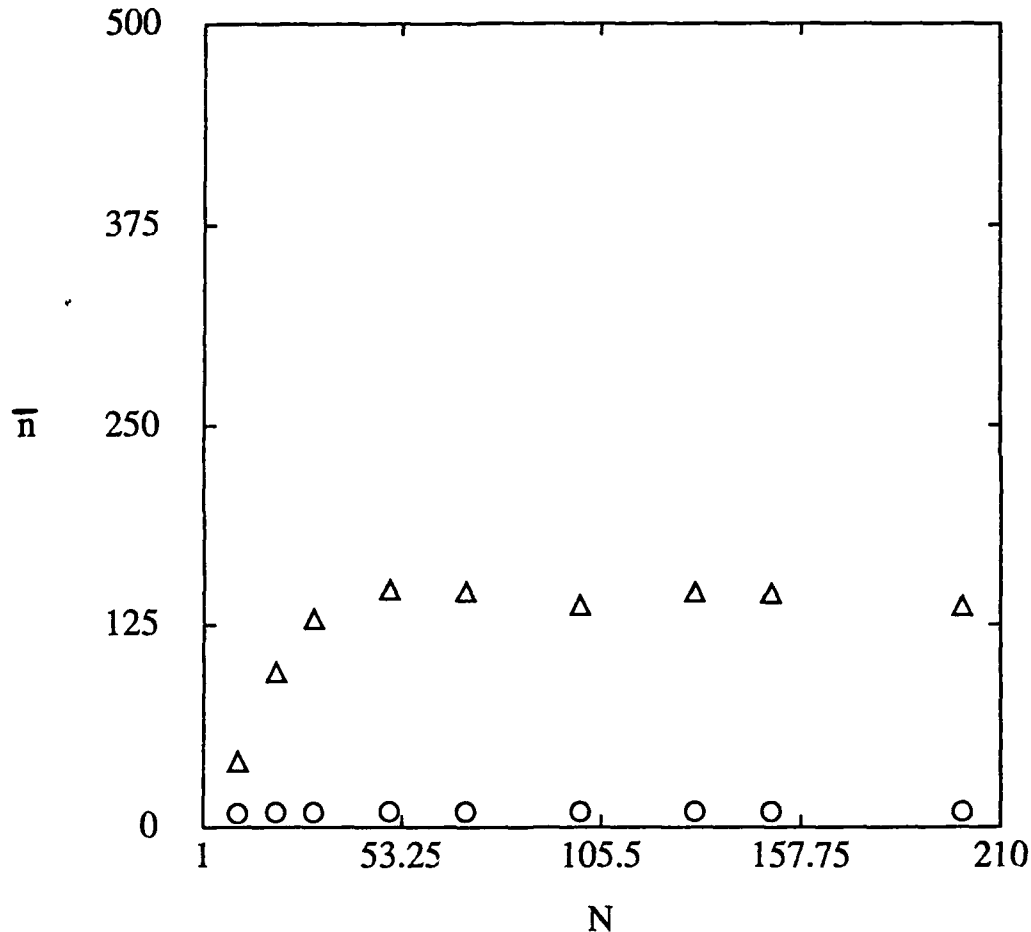


FIGURE 123. b Average number of iterations for the transient that take sloop1 to the final attractor for ring (square), double ring (triangle) and global coupling (circle) for $b = .1$ vs. number of loops for $\epsilon = .00001$

The state where the loops synchronize to a common frequency is stable for $0 < b_i < b^*$. When b_i is larger than b^* bifurcations and chaos appears. In a system with the same gain for all loops and $N \leq 200$ we observe the following: For the ring configuration the first bifurcation occurs always at $b^* = \Omega/\pi$ for any number of loops N . This result can be easily derived analytically for $N=2$, by performing a linear stability

analysis⁸. As N is increased we observe from the numerical simulations that this value remains the same. Just beyond the critical value b^* , there appears a periodic regime whose period is given by N^2 . This period refers to the number of samplings that makes the system return to a given state in frequency as well as in phase difference. By further increasing the gain more complex bifurcations occur which are followed by chaos.

For a double ring system the critical gain where the first bifurcation occurs is also given by $b^* = \Omega/\pi$, for N large. If N is odd and small, b^* differs from this value, converging to it as the size of the system increases, as shown in FIGURE 124.. As the gain increases beyond this critical value, there appears a bifurcation with period $2N$, where more than one basin of attraction is found for N sufficiently large. This bifurcation is followed by more complex bifurcations and then by a chaotic regime.

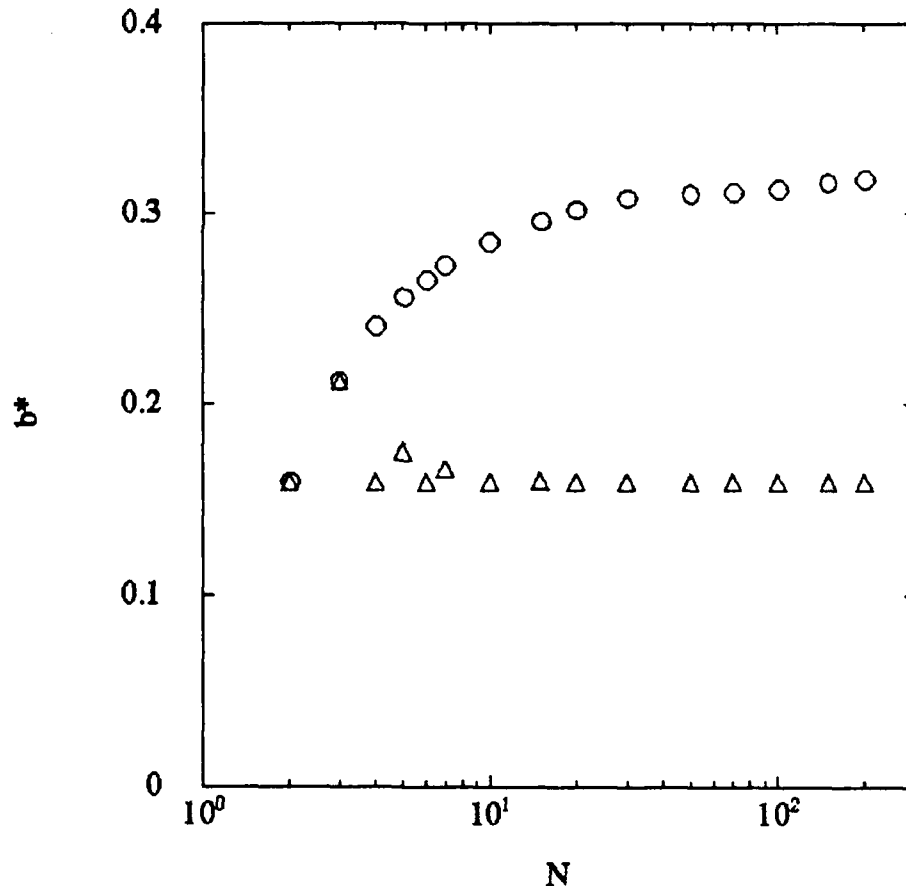


FIGURE 124. Critical value b^* which marks the upper border of stability for the synchronized regime in a double ring (triangle) and global coupling (circle)

In a global coupling configuration we find numerically that

b^* converges for large N to $b^*=2\Omega/\pi$, as seen in FIGURE 124. The attractor that follows the synchronized state has period $2N$ and has multiple basins of attraction, for N sufficiently large. Beyond this bifurcation more complex bifurcations appear as the gain is increased, which are followed by chaos. **Oscillators with different internal frequencies**

We now consider populations of DPLL's which have different internal frequencies. In this case, synchronization to a common frequency occurs over a range of the parameter space. The transition to the synchronized state is similar to the transition that occurs in the oscillators studied in ¹⁻⁴, which are governed by ODE's. For configurations where the communication between loops that are connected is in both directions, the synchronizing frequency is given by (87). Now, a phase difference between loops will occur at the synchronized state.

The synchronization is possible only if the gains b_i are large enough. Considering that $|\sin(\cdot)| \leq 1$, we obtain from (85)

$$\left| \frac{\omega_s - \Omega_i}{b_i/n_i} \right| \leq n_i \quad (89)$$

that is, for any i the relation $b_i \geq |\omega_s - \Omega_i|$ must be satisfied. Consider the case where the gains are the same for all loops, i.e., $b_i \equiv b$. We denote by b_c the critical value of b where the systems synchronize. From the above expressions, we find that the lower bound for b_c is given by $b = \max(|\omega_s - \Omega_i|)$. This expression holds for any configuration. As the gain b increases there will appear a bifurcation at a critical value b^* . The numerical calculations show that the critical value may be slightly greater than the b^* for the corresponding configuration with all the loops having the same center frequency. If the center frequencies are distributed over a large interval then synchronization may not be achieved. Suppose that they are distributed in the interval $1-\Delta \leq \Omega_i \leq 1+\Delta$. If Δ is larger than a critical value for which $b_c = b^*$, then the synchronized state cannot occur.

We did numerical simulations for the ring, double ring and global coupling geometries with Ω randomly distributed in the interval $[0.9;1.1]$, the gains being the same for all loops. First we calculated the transient to the locked state in the same way as we did for the system with identical center frequencies. The results for a system of $N=10$ and $b=0.16$ are shown in FIGURE 125. as a function of the accuracy ϵ . Here too

the transient \bar{n} is described by (88). As the gain increases the locked state becomes unstable and bifurcations are observed, which are followed by chaos.

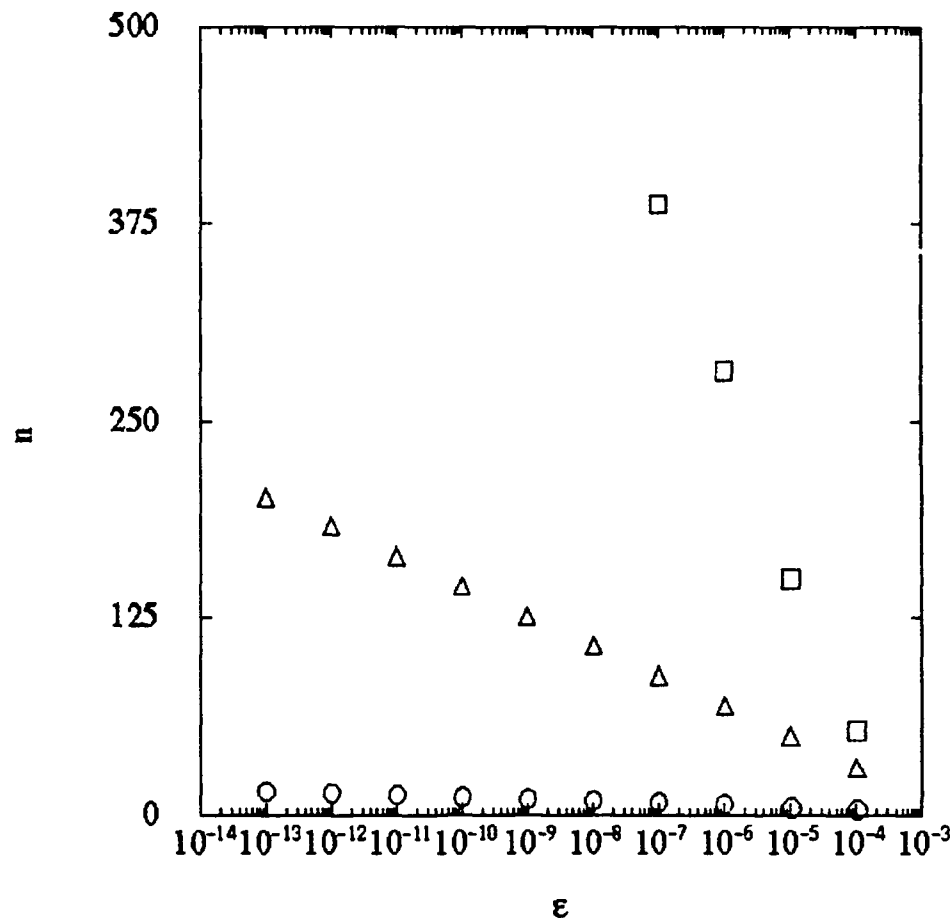


FIGURE 125. Average number of iterations for the transient that takes loop 1 to the final attractor for ring (square), double ring (triangle) and global coupling (circle for $b=0.16$ vs. ϵ with $N=10$)

3.9.4 CONCLUSIONS

We have shown that populations of nonuniformly sampled digital phase locked loops synchronize with a common frequency over a range of parameters. The synchronized frequency can be obtained analytically for configurations where the coupling between the connected loops occurs in both directions. In common with other coupled oscillator systems, if the spread in frequencies is not too large, there are transitions with increasing coupling from quasiperiodic to locked state and finally to chaos.

We studied the cases where the center frequencies are identical for all loops, and when they are spread. We found for both cases that the transient to the synchronized state and the parameter range where it is stable depend on the

configuration of the system, with the time to lock improving with the number of couplings for a fixed number of coupled devices N . The time to lock increases linearly with N for small N and approaches a constant value for large N . Among the geometries studied, global coupling showed the shortest transient to the locked state. This configuration also has the largest parameter region where the synchronization is possible.

3.9.5 REFERENCES

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